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1765

PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	10/099,972
Filing Date	March 19, 2002
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	1765
Examiner Name	D. Deo
Attorney Docket Number	0756-2457

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
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- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group (*Appeal Notice, Brief, Reply Brief*)
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosures
  1. Submission of Verification of Translation and JP 2001-091192
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Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

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Date	May 25, 2005

CERTIFICATE OF MAILING

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Attorney Docket No. 0756-2457

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 1765
Shunpei YAMAZAKI et al.	)	Examiner: D. Deo
Serial No. 10/099,972	)	
Filed: March 19, 2002	)	
For: WIRING AND METHOD OF	)	
MANUFACTURING THE SAME, AND	)	
WIRING BOARD AND METHOD OF	)	
MANUFACTURING THE SAME	)	

CERTIFICATE OF MAILING

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Adele M Stamper

SUBMISSION OF VERIFICATION OF TRANSLATION

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Further to the Response filed on May 9, 2005, submitted herewith is an English translation of JP 2001-091192 filed on March 27, 2001. Since JP 11-264101 has a filing date of March 30, 2001, which is later than the filing date of JP 2001-091192, the Applicants respectfully submit that any potential rejections under §§ 102 and 103 should be overcome.

Respectfully submitted,

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Docket No.: 0756-2457

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)
Shunpei YAMAZAKI et al.	)
Application No.: 10/099,972	) Examiner: D. Deo
Filed: March 19, 2002	) Group Art Unit: 1765
For: WIRING AND METHOD OF MANUFACTURING	)
THE SAME, AND WIRING BOARD AND METHOD OF	)
MANUFACTURING THE SAME	)
	)

VERIFICATION OF TRANSLATION

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

I, Satoru Okamoto, C/O Semiconductor Energy Laboratory Co., Ltd. 398, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, herewith declare:

that I am well acquainted with both the Japanese and English Languages; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 2001-091192 filed on March 27, 2001.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 20 day of May

S. Okamoto

Name: Satoru Okamoto

[Name of Document] Patent Application
[Reference Number] P005628
[Filing Date] March 27, 2001
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[Indication of Handlings]
[Number of Prepayment Note] 002543
[Payment Amount] ¥ 21,000
[List of Attachment]

[Attachment]	Specification	1
[Attachment]	Drawing	1
[Attachment]	Abstract	1
[Proof]	required	

[Name of Document] Specification

[Title of Invention] **WIRING AND METHOD OF MANUFACTURING THE SAME, AND WIRING BOARD AND METHOD OF MANUFACTURING THE SAME**

[Scope of Claim]

[Claim 1] A wiring characterized in that having a layered structure including a first conductive layer with a first width as a first layer, a second conductive layer with a second width smaller than said first width as a second layer, and a third conductive layer with a third width smaller than said second width as a third layer.

[Claim 2] A wiring having a layered structure including a first conductive layer with a first width as a first layer, a second conductive layer with a second width smaller than said first width as a second layer, and a third conductive layer with a third width smaller than said second width as a third layer,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 3] According to Claim 1 or 2, a wiring characterized in that said first conductive layer has a conductive layer made of one or a plurality of kinds of elements selected from W and Mo, or an alloy or compound mainly containing one or the plurality of kinds of elements selected from W and Mo.

[Claim 4] According to Claim 1 or 2, a wiring characterized in that said second conductive layer has a conductive layer made of an alloy or compound mainly containing Al.

[Claim 5] According to Claim 1 or 2, a wiring characterized in that said third conductive layer has a conductive layer made of an alloy or compound mainly containing Ti.

[Claim 6] In either of Claims from 1 to 5, a wiring wherein said second conductive layer is covered with said first conductive layer, said third conductive layer, and insulating film,

characterized in that:

a region contacting said insulating film is oxidized.

[Claim 7] In either of Claim from 1 to 6, a wiring characterized in that said wiring has a liquid crystal display device or a light-emitting device.

[Claim 8] A method of manufacturing a wiring characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width; and

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with said second width, and a third conductive layer with said third width.

[Claim 9] A method of manufacturing a wiring characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive

layer comprising a lamination of the first conductive layer with the fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width.

[Claim 10] A method of manufacturing a wiring comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width; and

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 11] A method of manufacturing a wiring comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with said fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 12] A method of manufacturing a wiring characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

a step of conducting plasma treatment to said third-shaped conductive layer.

[Claim 13] A method of manufacturing a wiring characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped

conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width;

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with said fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width; and

a step of conducting a plasma treatment to said fourth-shaped conductive layer.

[Claim 14] A method of manufacturing a wiring comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

a step of conducting plasma treatment to said third-shaped conductive layer,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 15] A method of manufacturing a wiring comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width;

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with said fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width; and

a step of conducting a plasma treatment to said fourth-shaped conductive layer,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 16] In either of Claims from 8 to 15, a method of manufacturing a wiring characterized in that said first conductive layer has a conductive layer made of one or a plurality of kinds of elements selected from W and Mo, or an alloy or compound mainly containing one or the plurality of kinds of elements selected from W and Mo.

[Claim 17] In either of Claims from 8 to 15, a method of manufacturing a wiring characterized in that said second conductive layer has a conductive layer made of an alloy or compound mainly containing Al.

[Claim 18] In either of Claims from 8 to 15, a method of manufacturing a wiring characterized in that said third conductive layer has a conductive layer made of an alloy or compound mainly containing Ti.

[Claim 19] In either of Claims from 12 to 15, a method of manufacturing a

wiring characterized in that said plasma treatment is conducted by using oxygen or a gas mainly containing oxygen, or H_2O.

[Claim 20] In either of Claims from 12 to 19, a method of manufacturing a wiring characterized in that said wiring has a liquid crystal display device or a light-emitting device.

[Claim 21] In a wiring board having an insulating substrate and a wiring, a wiring characterized in that said wiring has a layered structure including a first conductive layer with a first width as a first layer, a second conductive layer with a second width smaller than said first width as a second layer, and a third conductive layer with a third width smaller than said second width as a third layer.

[Claim 22] In a wiring board having an insulating substrate and a wiring, a wiring board wherein said wiring has a layered structure including a first conductive layer with a first width as a first layer, a second conductive layer with a second width smaller than said first width as a second layer, and a third conductive layer with a third width smaller than said second width as a third layer,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 23] In Claim 21 or 22, a wiring board characterized in that said first conductive layer has one or a plurality of kinds of elements selected from W and Mo, or an alloy material or compound material mainly containing one or the plurality of kinds of elements selected from W and Mo.

[Claim 24] In Claim 21 or 22, a wiring board characterized in that said second conductive layer has an alloy material or compound material mainly containing Al.

[Claim 25] In Claim 21 or 22, a wiring board characterized in that said third conductive layer has an alloy material or compound material mainly containing Ti.

[Claim 26] In either of Claims from 21 to 25, a wiring board wherein said second conductive layer is covered with said first conductive layer, said third conductive layer, and an insulating film,

characterized in that:

a region contacting said insulating film is oxidized.

[Claim 27] In either of Claims from 21 to 26, a wiring characterized in that a liquid crystal display device or a light-emitting device is manufactured by using said wiring board.

[Claim 28] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first conductive layer on an insulating surface;

a step of forming a second conductive layer on said first conductive layer;

a step of forming a third conductive layer on said second conductive layer; and

etching from said first conductive layer to third conductive layer, a step of forming a conductive layer having a taper shape.

[Claim 29] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by forming a wiring comprising: a fist conductive layer with a first width on an insulating surface; a second conductive layer with a second width; and a third conductive layer with a third width.

[Claim 30] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by forming a wiring comprising: a fist conductive layer with a first width on an insulating surface; a second conductive layer with a second width; and a third conductive layer with a third width,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 31] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a

first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width; and

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width.

[Claim 32] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width; and

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width,

characterized in that:

a cross-section of edges of a first conductive layer with said fourth width, a second conductive layer with said second width, or a third conductive layer with a third width has a taper shape.

[Claim 33] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with the fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width.

[Claim 34] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

etching the second conductive layer with said second width and the third

conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with the fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width,

characterized in that:

a cross-section of edges of a first conductive layer with said fourth width, a second conductive layer with said fifth width, or a third conductive layer with a six width has a taper shape.

[Claim 35] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first conductive layer on an insulating surface;

a step of forming a second conductive layer on said first conductive layer;

a step of forming a third conductive layer on said second conductive layer;

etching from said first conductive layer to third conductive layer, a step of forming a conductive layer having a taper shape; and

a step of conducting a plasma treatment to a conductive layer having said taper shape.

[Claim 36] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a conductive layer comprising a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width on an insulating surface; and

a step of conducting a plasma treatment to said conductive layer.

[Claim 37] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by comprising:

a step of forming a conductive layer comprising a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width on an insulating surface; and

a step of conducting a plasma treatment to said conductive layer,

characterized in that:

a cross-section of edges of said first conductive layer, said second conductive layer, or said third conductive layer has a taper shape.

[Claim 38] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width; and

a step of conducting plasma treatment to said third-shaped conductive layer.

[Claim 39] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth

width, the second conductive layer with said second width, and the third conductive layer with said third width; and

a step of conducting a plasma treatment to said third-shaped conductive layer, characterized in that:

a cross-section of edges of a first conductive layer with said fourth width, a second conductive layer with said second width, or a third conductive layer with a first width has a taper shape.

[Claim 40] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board characterized by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width;

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with the fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width; and

a step of conducting plasma treatment to said fourth-shaped conductive layer.

[Claim 41] In a method of manufacturing a wiring board having an insulating substrate and a wiring, a method of manufacturing a wiring board by comprising:

a step of forming a first-shaped conductive layer comprising a lamination of a

first conductive layer with a first width, a second conductive layer, and a third conductive layer on an insulating surface;

etching said second conductive layer and said third conductive layer, a step of forming a second-shaped conductive layer comprising a lamination of the first conductive layer with said first width, the second conductive layer with a second width, and the third conductive layer with a third width;

etching said first conductive layer, a step of forming a third-shaped conductive layer comprising a lamination of the first conductive layer with a fourth width, the second conductive layer with said second width, and the third conductive layer with said third width;

etching the second conductive layer with said second width and the third conductive layer with said third width, a step of forming a fourth-shaped conductive layer comprising a lamination of the first conductive layer with the fourth width, the second conductive layer with a fifth width, and the third conductive layer with a sixth width; and

a step of conducting plasma treatment to said fourth-shaped conductive layer,

characterized in that:

a cross-section of edges of a first conductive layer with said fourth width, a second conductive layer with said fifth width, or a third conductive layer with a six width has a taper shape.

[Claim 42] In either of Claims from 28 to 41, a wiring board characterized in that said first conductive layer has one or a plurality of kinds of elements selected from W and Mo, or an alloy material or compound material mainly containing one or the plurality of kinds of elements selected from W and Mo.

[Claim 43] In either of Claims from 28 to 41, a method of manufacturing a wiring board characterized in that said second conductive layer has a conductive layer made of an alloy material or compound material mainly containing Al.

[Claim 44] In either of Claims from 28 to 41, a method of manufacturing a wiring board characterized in that said third conductive layer has a conductive layer made of an alloy material or compound material mainly containing Ti.

[Claim 45] In either of Claims from 35 to 41, a method of manufacturing a wiring board characterized in that said plasma treatment is conducted by using oxygen or a gas mainly containing oxygen, or H_2O.

[Claim 46] In either of Claims from 28 to 45, a method of manufacturing a wiring board characterized in that a liquid crystal display device or a light-emitting device is manufactured by using said wiring board.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

The present invention relates to wiring formed by using a thin film technique and a method of manufacturing the same. The present invention also relates to a wiring board and a method of manufacturing the same. In the present specification, a wiring board refers to an insulating substrate made of glass, etc. or various substrates having wiring formed by using a thin film technique.

[0002]

[Prior Art]

In recent years, a technique of forming a thin film transistor (TFT) using a semiconductor thin film (thickness of about from several to hundreds of nm) formed on a substrate having an insulating surface has been paid attention to. A TFT is widely applied to an electronic device such as an integrated circuit (IC) and an electrooptic apparatus. In particular, a TFT is being rapidly developed as a switching element of an image display apparatus.

[0003]

Conventionally, a liquid crystal display device is known as an image display apparatus. Since an image of higher precision can be obtained compared with a passive type liquid crystal display device, an active matrix type liquid crystal display device is being used more. In an active matrix type liquid crystal display device, pixel electrodes arranged in matrix are driven, whereby a display pattern is formed on a screen. More specifically, a voltage is applied between a selected

pixel electrode and a counter electrode corresponding to the pixel electrode, whereby a liquid crystal layer disposed between the pixel electrode and the counter electrode is subjected to optical modulation, and this optical modulation is recognized as a display pattern by an observer.

[0004]

Such an active matrix type liquid crystal display device has a wider range of uses, and there is an increasing demand for high precision, a high aperture ratio, and high reliability, as well as enlargement of a screen size. There is also a demand for enhancement of productivity and a decrease in cost.

[0005]

[Problem to be Solved by the Invention]

In the case where aluminum (Al) is used as wiring of the above-mentioned TFT in order to manufacture TFT, projections such as hillock and whisker are formed due to a heat treatment, and an Al atom diffuses to an insulating film and an active region (in particular, a channel-formation region), which may cause operation defects of the TFT or a decrease in electrical characteristics of the TFT.

[0006]

Under such a circumstance, the use of a metal material withstanding a heat treatment (typically, a metal element having a high melting point, such as tungsten (W) and molybdenum (Mo)) is considered. However, the resistivity of these elements is very high compared with that of Al (see Table 1).

[0007]

[Table 1]

wiring material	resistivity [μΩcm]
Al	2
W	10～20
Mo	15～25

[0008]

Therefore, when a screen size is enlarged, a wiring delay becomes a problem. In view of this, a method for decreasing a resistance by making wiring thicker is

considered. However, when the width of wiring is enlarged, a degree of design freedom and an aperture ratio in a pixel portion may be lowered, which will be a problem. Furthermore, when the film thickness of wiring is made larger, a short-circuit is likely to be caused at a portion where wiring crosses to each other three-dimensionally, and coverage is degraded at a step difference portion of the wiring.

[0009]

A problem of the present invention is, therefore, to provide a wiring that is ready for enlargement of a screen and a method of manufacturing the same, and a wiring board and a method of manufacturing the same.

[0010]

[Means for Solving the Problem]

According to the present invention, wiring has a layered structure that includes: as a first layer, a conductive film mainly containing one or a plurality of kinds of elements selected from W and Mo, or one or a plurality of kinds of elements selected from W and Mo; as a second layer, a low-resistant conductive film mainly containing Al; and as a third layer, a conductive film mainly containing Ti, whereby it is attempted to lower a resistance of wiring. According to the present invention, the low-resistant conductive film mainly containing Al is sandwiched with other conductive films, whereby formation of projections such as hillock and whisker due to a heat treatment can be prevented. Furthermore, since the first and third layers are made of conductive films with a high melting point, they function as barrier metal, which can prevent an Al atom from diffusing to an insulating film and an active region (Table 2). Furthermore, when an insulating film is formed on wiring of the present invention and contact with the wiring is formed, the third layer functions as a stopper for etching of said insulating film, so that contact can be easily formed. When Al comes into contact with an ITO film typical as transparent conductive film, Al causes electric corrosion to increase a contact resistance. However, the third layer is made of a conductive film mainly containing Ti, so that the contact resistance becomes satisfactory.

[0011]

[Table 2]

wiring material	melting point [°C]
Al	660.4
W	3387
Mo	2610
Ti	1675

[0012]

Furthermore, according to the present invention, at least edges of the second layer made of a low-resistant conductive film mainly containing Al have a taper shape. Because of the taper shape, coverage at the step difference portion is enhanced. In the present specification, a taper angle refers to an angle formed by a horizontal surface and a side surface of a material layer. Furthermore, in the present specification, for convenience sake, the side surface with a taper angle is referred to as a taper shape, and a portion with a taper shape is referred to as a taper portion.

[0013]

A constitution of the present invention disclosed in the present specification relates to wiring characterized by having a layered structure including a first conductive layer with a first width as a first layer, a second conductive layer with a second width smaller than said first width as a second layer, and a third conductive layer with a third width smaller than said second width as a third layer.

[0014]

In the above-mentioned constitution, said wiring is characterized by having a layered structure that includes a conductive layer (first layer) made of an alloy or a compound mainly containing W, a conductive layer (second layer) made of an alloy or a compound mainly containing Al, and a conductive layer (third layer) made of an alloy or a compound mainly containing Ti. Alternatively, said wiring is characterized by having a layered structure that includes a conductive layer (first layer) made of an alloy or a compound mainly containing Mo, a conductive layer

(second layer) made of an alloy or a compound mainly containing Al, and a conductive layer (third layer) made of an alloy or a compound mainly containing Ti. For example, as the first layer, W, WN, Mo, or the like can be used. As the second layer, Al, Al–Si (2 wt%), Al–Ti (1 wt%), Al–Nd (1 wt%), Al–Sc (0.18 wt%), or the like can be used. As the third layer, Ti, TiN, or the like can be used. These layers can be formed by sputtering method, plasma CVD method, or the like. Furthermore, when Al–Si or the like is formed in the second layer, there is a limit (solid solubility limit) to the ratio at which an element such as Si can dissolve in Al. The higher the solution degree is, the more a resistivity is increased, and heat resistance is also changed. Therefore, those skilled in the art may appropriately determine the ratio of Si or the like to Al, depending upon the resistivity and heat resistance suitable for wiring, and the solid solubility limit of an element such as Si.

[0015]

Table 3 shows examples of a resistivity in each conductive layer that constitutes wiring. It is understood from Table 3 that a conductive layer made of an alloy or a compound mainly containing Al has a very low resistance, compared with the other conductive layers.

[0016]

[Table 3]

wiring material		resistivity [μΩcm]
material mainly containing W	W	10～20
	WN	150～220
material mainly containing Al	Al	2
	Al-Si (2 wt%)	3.5～4.5
	Ai-Ti (1 wt%)	8～10
	Al-Nd (1 wt %)	7～10
	Al-Sc (0.18 wt%)	3.5～4.0
material mainly containing Ti	Ti	50～60
	TiN	130～200

[0017]

Any etching method can be applied, as long as the first, second, and third conductive films having heat resistance and conductivity can be etched at a high speed with good precision, and furthermore, edges of the films can be tapered. Among them, in particular, a dry etching method using high-density plasma is desirably used. An etching apparatus using a microwave, helicon wave plasma (HWP), or inductively coupled plasma (ICP) is suitable for a procedure of obtaining high-density plasma. For example, an electron cyclotron resonance (ECR) etching apparatus, a surface wave plasma (SWP) etching apparatus, an ICP etching apparatus, a two-frequency parallel-plate excitation-type etching apparatus, or the like may be used. In particular, the ICP etching apparatus controls plasma easily, and is ready for enlargement of a substrate to be treated.

[0018]

For example, as a method to conduct a plasma treatment with high precision, a method of forming plasma by applying a high-frequency electric power to a multi-spiral coil in which a plurality of spiral coil portions are connected in parallel via an impedance matching circuit is used. Furthermore, a high-frequency electric power is also applied to a lower electrode holding a substance to be treated, thereby supplying a bias voltage thereto.

[0019]

When the ICP etching apparatus adopting such a multi-spiral coil is used, a taper angle is substantially varied depending upon a bias electric power applied to a substrate side. Therefore, by further increasing a bias electric power and changing a pressure, a taper angle can be changed in a range of from 5° to 85°.

[0020]

As gas used for etching the second and third layers, a chlorine-based gas is desirable. For example, $SiCl_4$, HCl, CCl_4, BCl_3, Cl_2, or the like can be used.

[0021]

As gas used for etching the first layer, fluorine-based gas is desirable. For example, NF_3, CF_4, C_2F_6, SF_6, or the like can be used. When a chlorine gas is introduced simultaneously with a fluorine gas, an etching rate in the first layer is

enhanced, which is desirable.

[0022]

Furthermore, by allowing the wiring to have a layered structure using the above-mentioned conductive layers, the edges of the wiring are tapered by using an ICP etching method or the like. By tapering the edges of the wiring, coverage of films to be formed in the later processes can be made satisfactory.

[0023]

In the above-mentioned constitution, the edges of said first conductive layer have taper shape. A portion having the taper shape (i.e., a taper portion) is a region that is not overlapped with the second conductive layer, and the width of the region corresponds to that obtained by subtracting the second width from the first width. The second conductive layer is also tapered, but the taper angle thereof is made larger than that of the taper portion of the first conductive layer. Furthermore, the third conductive layer is also tapered, but the taper angle thereof is made substantially the same as that of the taper portion of the second conductive layer.

[0024]

The constitution for realizing the present invention relates to a method of a manufacturing wiring corresponding: a step of forming a wiring on an insulating surface; and a step of etching said wiring to form a taper shape.

[0025]

In the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive film mainly containing W, forming a conductive film mainly containing Al, and forming a conductive film mainly containing Ti are stacked on top of each other, followed by etching with a mask. Furthermore, in the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive layer mainly containing Mo, forming a conductive layer mainly containing Al, and forming a conductive layer mainly containing Ti are stacked on top of each other, followed by etching with a mask.

[0026]

The other constitution for realizing the present invention relates to a method

of manufacturing wiring corresponding: a step of forming a multilayer film that is stacked on top of each other on an insulating surface in the order of a first conductive layer, a second conductive layer, and a third conductive layer; and a step of etching said multilayer film to form a taper shape.

[0027]

In the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive film mainly containing W, forming a conductive film mainly containing Al, and forming a conductive film mainly containing Ti are stacked on top of each other, followed by etching with a mask. Furthermore, in the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive layer mainly containing Mo, forming a conductive layer mainly containing Al, and forming a conductive layer mainly containing Ti are stacked on top of each other, followed by etching with a mask.

[0028]

The other constitution of the present invention disclosed in the present specification, in a wiring board having an insulating substrate and wiring, relates to a wiring board, characterized in that said wiring having a layered structure including: a first conductive layer with a first width as a first layer; a second conductive layer with a second width smaller than the first width as a second layer; and a third conductive layer with a third width smaller than the second width as a third layer.

[0029]

In the above-mentioned constitution, said wiring is comprising a layered structure including: a conductive layer (first layer) made of an alloy or a compound mainly containing W; a conductive layer (second layer) made of an alloy or a compound mainly containing Al; and a conductive layer (third layer) made of an alloy or a compound mainly containing Ti. Alternatively, said wiring is comprising a layered structure including: a conductive layer (first layer) made of an alloy or a compound mainly containing Mo; a conductive layer (second layer) made of an alloy or a compound mainly containing Al; and a conductive layer (third layer)

made of an alloy or a compound mainly containing Ti.

[0030]

Furthermore, by allowing the wiring to have a layered structure using the above-mentioned conductive layers, the edges of the wiring are tapered by using an ICP (Inductively Coupled Plasma) etching method or the like. By tapering the edges of the wiring, coverage of films to be formed in the later processes can be made satisfactory.

[0031]

In the above-mentioned constitution, the edges of the first conductive layer are desirably tapered. A portion having a taper shape (i.e., a taper portion) is a region that is not overlapped with the second conductive layer, and the width of the region corresponds to that obtained by subtracting the second width from the first width. It is also desirable that the second conductive layer is tapered, and the taper angle thereof is made larger than that of the taper portion of the first conductive layer. Furthermore, it is desirable that the third conductive layer is tapered, and the taper angle thereof is made substantially the same as that of the taper portion of the second conductive layer.

[0032]

The constitution for realizing the present invention, in a method of manufacturing a wiring board having an insulating substrate and wiring, relates to a method of manufacturing a wiring board comprising: a step of forming a wiring on an insulating surface; and a step of etching said wiring to form a taper shape.

[0033]

In the above-mentioned constitution, a step of forming said wiring is comprising a conductive film mainly containing W, forming a conductive film mainly containing Al, and forming a conductive film mainly containing Ti are stacked on top of each other, followed by etching with a mask. Furthermore, in the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive layer mainly containing Mo, forming a conductive layer mainly containing Al, and forming a conductive layer mainly containing Ti are

stacked on top of each other, followed by etching with a mask.

[0034]

The other constitution for realizing the present invention, in a method of manufacturing a wiring board having an insulating substrate and wiring, relates to a method of manufacturing a wiring board comprising: a step of forming a multilayer film that is stacked on top of each other on an insulating surface in the order of a first conductive layer, a second conductive layer, and a third conductive layer; and a step of etching said multilayer film to form a taper shape.

[0035]

In the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive film mainly containing W, forming a conductive film mainly containing Al, and forming a conductive film mainly containing Ti are stacked on top of each other, followed by etching with a mask. Furthermore, in the above-mentioned constitution, a step of forming said wiring is characterized in that forming a conductive layer mainly containing Mo, forming a conductive layer mainly containing Al, and forming a conductive layer mainly containing Ti are stacked on top of each other, followed by etching with a mask.

[0036]

[Embodiment modes of the Invention]

An embodiment of the present invention will be described with reference to FIG 1. In the present embodiment, a wiring board provided with a gate electrode of a TFT utilizing the present invention will be described.

[0037]

First, a base insulating film 11 is formed on a substrate 10. As the substrate 10, a glass substrate, a quartz substrate, a silicon substrate, or a substrate an insulating film is formed on a metal substrate or on a surface of a stainless steal substrate may be also used. Furthermore, a plastic substrate may be also employed when it has a heat resistance against the process temperature.

[0038]

Furthermore, as the base insulating film 11, a base film 11 made of an

insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed. Herein, the base film 11 with a double-layered structure (11a, 11b) was exemplified; however, the base film 11 may also be formed from a single-layered film of said insulating film or a multi-layered structure of two or more layers. Note that the base insulating film may not need to be formed.

[0039]

Then, a semiconductor layer 12 is formed on the base insulating film. The semiconductor layer 12 is obtained by forming a semiconductor film having an amorphous structure by a known method (sputtering method, LPCVD method, plasma CVD method, etc.), followed by patterning a crystalline semiconductor film obtained by conducting a known crystallization treatment (laser crystallization method, thermal crystallization method, thermal crystallization method using a catalyst such as nickel, etc.) into a desired shape using a first photomask. The semiconductor layer 12 is formed to have a thickness of from 25 to 80 nm (preferably, from 30 to 60 nm). There is no particular limit to a material for the crystalline semiconductor film; however, the crystalline semiconductor film may be preferably formed of silicon, a silicon-germanium (SiGe) alloy, or the like.

[0040]

Then, an insulating film 13 is formed so as to cover the semiconductor layer 12. The insulating film 13 is formed using plasma CVD method or sputtering method to have a thickness of from 40 to 150 nm so as to have a single-layered structure or a multi-layered structure of an insulating film containing silicon. Note that the insulating film 13 is to be a gate insulating film.

[0041]

Next, a first conductive film 14 with a thickness of from 20 to 100 nm, a second conductive film 15 with a thickness of from 100 to 800 nm, and a third conductive film 16 with a thickness of from 20 to 100 nm are layered on the insulating film 13. Herein, these conductive films may be formed using sputtering method, plasma CVD method, or the like, and as the first conductive film contacting with the insulating film, a conductive film (W, WMo, Mo, etc.) mainly containing W

or Mo may be used so as to prevent diffusion to a channel formation region. Furthermore, as the second conductive film, a low-resistant conductive film (Al, Al–Ti, Al–Sc, Al–Si, etc.) mainly containing Al may be used. As the third conductive film, a conductive film (Ti, TiN, etc.) mainly containing Ti with a low contact resistance may be used.

[0042]

Then, a resist mask 17a is formed using a second photomask, and a first etching process is conducted using an inductively coupled plasma (ICP) etching apparatus or the like. Due to the first etching process, from the first to third conductive films from 15 to 16 are etched to obtain conductive layers from 18a to 20a having taper portions at edges as shown in FIG. 1B.

[0043]

A second etching process is conducted in an ICP etching apparatus, using the resist mask 16a formed in a second photolithography process as it is. Due to the second etching process, the second conductive layer 19a and the third conductive layer 18a are selectively etched to obtain a second conductive layer 19b and a third conductive layer 18b as shown in FIG. 1C. Note that, during the second etching, the resist mask, the first conductive layer, and the insulating film are slightly etched to form a resist mask 17b, the first conductive layer 20b, and an insulating film 22b. The first conductive layer 20b has a first width (W1), the second conductive layer 19b has a second width (W2), and the third conductive layer 18b has a third width (W3). Note that the first width is larger than the second width, and the second width is larger than the third width.

[0044]

Herein, in order to suppress film reduction of the insulating film 13, etching was conducted twice (first and second etching processes). However, as long as an electrode structure (layered structure of the second conductive layer 17b and the first conductive layer 18a) as shown in FIG. 2C can be formed, there is no particular limit. Etching may be also conducted once.

[0045]

As described above, according to the present invention, a gate line is formed of low-resistant conductive layers. Therefore, even if the area of a pixel portion is enlarged, the pixel can be sufficiently driven. Needless to say, the present invention is applicable to various wiring as well as a gate line, and a wiring board with the wiring formed thereon can be manufactured.

[0046]

The present invention with the above-mentioned constitution will be described in detail by way of the following embodiments.

[0047]

[Embodiments of the Invention]

The embodiments of the present invention will be described below; however, it should be noted that the present invention is not limited thereto.

[0048]

[Embodiment 1]

An exemplary structure of a wiring board provided with a gate electrode using the present invention will be described below.

[0049]

First, a base insulating film 11 is formed on a substrate 10. As the substrate 10, a glass substrate, a quartz substrate, a silicon substrate, or a substrate an insulating film is formed on a metal substrate or on a surface of a stainless steal substrate may be also used. Furthermore, a plastic substrate may also be employed when it has a heat resistance against the process temperature. In the present embodiment, a glass substrate 1737 produced by Corning Co. was used.

[0050]

Furthermore, as the base insulating film 11, a base film 11 made of an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed. Herein, the base film 11 with a double-layered structure (11a, 11b) was exemplified; however, the base film 11 may also be formed from a single-layer film of said insulating film or a multi-layered structure of two or more layers. Note that the base insulating film may not need to be formed. In the

present embodiment, a silicon oxynitride film 11a with a thickness of 50 nm (composition ratio: Si = 32%, O = 27%, N = 24%, H = 17%) was formed. Then, a silicon oxynitride film 11b with a thickness of 100 nm (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) was formed.

[0051]

Then, a semiconductor layer 12 is formed on the base insulating film. The semiconductor layer 12 is obtained by forming a semiconductor film with an amorphous structure by a known method (sputtering method, LPCVD method, plasma CVD method, etc.), followed by patterning a crystalline semiconductor film obtained by conducting a known crystallization treatment (laser crystallization method, thermal crystallization method, thermal crystallization method using a catalyst such as nickel, etc.) into a desired shape using a first photomask. The semiconductor layer 12 is formed to have a thickness of from 25 to 80 nm (preferably, 30 to 60 nm). There is no particular limit to a material for the crystalline semiconductor film; however, the crystalline semiconductor film may be preferably formed of silicon, a silicon-germanium (SiGe) alloy, or the like. In the present embodiment, an amorphous silicon film was formed to have a thickness of 55 nm using plasma CVD, and then, a solution containing nickel was held on the amorphous silicon film. The amorphous silicon film was dehydrogenated at 500°C for an hour, and subjected to thermal crystallization at 550°C for 4 hours. In addition, a laser annealing treatment for improving crystallization was conducted to form a crystalline silicon film. The crystalline silicon film was conducted a patterning treatment using photolithography method to form a semiconductor layer 12.

[0052]

Then, an insulating film 13 is formed so as to cover the semiconductor layer 12. The insulating film 13 is formed using plasma CVD method or sputtering method to have a thickness of from 40 to 150 nm so as to have a single-layered structure or a multi-layered structure of an insulating film containing silicon. Note that, the insulating film 13 is to be a gate insulating film. In the present

embodiment, a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) was formed to have a thickness of 110 nm by plasma CVD method.

[0053]

Next, a first conductive film 14 with a thickness of from 20 to 100 nm, a second conductive film 15 with a thickness of from 100 to 800 nm, and a third conductive film 16 with a thickness of from 20 to 100 nm are layered on the insulating film 13. These conductive films may be formed by sputtering method or the like, and as the first conductive film contacting with the insulating film, a conductive film (W, WMo, Mo, etc.) mainly containing W or Mo may be used so as to prevent diffusion to a channel-formation region. Furthermore, as the second conductive film, a low-resistant conductive film (Al, Al–Ti, Al–Sc, Al–Si, etc.) mainly containing Al may be used. As the third conductive film, a conductive film mainly containing Ti (Ti, TiN, etc.) with a low contact resistance may be used. In the present embodiment, a first conductive film 14 made of a W film with a thickness of 30 nm, a second conductive film 15 made of an Al–Ti film with a thickness of 500 nm, and a third conductive film 16 made of a Ti film with a thickness of 50 nm were layered by sputtering method. The ratio of Ti of the second conductive film 15 was 1%, and the second conductive film 15 was formed using Al-Ti as a target.

[0054]

Then, a first etching treatment is conducted. The first etching treatment is conducted under a first etching condition and a second etching condition. In the present embodiment, as the first etching condition, an ICP (Inductively Coupled Plasma) etching method was used. More specifically, etching was conducted for 147 seconds, using BCl_2, Cl_2, and O_2 as an etching gas in a gas flow rate of 65/10/5 (sccm) and with an RF (13.56 MHz) power of 450 W supplied to a coil-shaped electrode under a pressure of 1.2 Pa to generate plasma. Herein, a dry etching apparatus (Model E645– □ ICP) using ICP produced by Matsushita Electric Industrial Co., Ltd. was used. An RF (13.56 MHz) power of 300 W is also supplied to a substrate side (sample stage), whereby a substantially negative

self-bias voltage is applied thereto. Under the first etching condition, an etching speed with respect to the resist is 235.5 nm/min, an etching speed with respect to Al–Ti is 233.4 nm/min, and an etching speed with respect to W is 133.8 nm/min. Under the first etching condition, the Al–Ti film and the Ti film are etched to taper the edges of second and third conductive layers. Furthermore, under the first etching condition, the taper angle of the Al–Ti film and the Ti film becomes about 45°.

[0055]

Thereafter, the etching condition is changed to the second etching condition without removing a resist mask 17a. Under the second etching condition, etching was conducted for 30 seconds, using CF_4, Cl_2, and O_2 as an etching gas in a gas flow rate of 25/25/10 (sccm) and with an RF (13.56 MHz) power of 500 W supplied to a coil-shaped electrode under a pressure of 1 Pa to generate plasma. An RF (13.56 MHz) power of 20 W is also supplied to a substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. Under the second etching condition in which CF_4, Cl_2, and O_2 are mixed, only the W film is etched. The etching speed with respect to W under the second etching condition is 124.6 nm/min. Note that, in order to conduct etching without leaving a residue on a gate insulating film, it is preferable that an etching time may be increased by about from 10 to 20%.

[0056]

In the above-mentioned first etching process, by making the shape of a resist mask appropriate, the edges of the first and second conductive layers are tapered due to the effect of a bias voltage applied to the substrate side. The taper angle may be set to be from 15° to 45°. Accordingly, a first-shaped conductive layer composed of a first conductive layer 20a, a second conductive layer 19a, and a third conductive layer 18a is formed by the first etching treatment. The width of the first conductive layer in a channel length direction herein corresponds to W1 shown in the above-mentioned embodiment mode. Reference numeral 21a denotes a gate insulating film, and regions not covered with a first-shaped conductive layer are

slightly etched by about from 20 to 50 nm to form a thin region. Note that the second etching treatment herein corresponds to the first etching process (FIG. 1B) described in the above-mentioned embodiment mode. FIG. 2A shows an SEM photograph of the first-shaped conductive layer thus formed.

[0057]

Then, a second etching treatment is conducted without removing a resist mask. Herein, etching was conducted, using BCl_3 and Cl_2 as an etching gas in a gas flow rate of 20/60(sccm) and with an RF (13.56 MHz) power of 600 W supplied to a coil-shaped electrode under a pressure of 1.2 Pa to generate plasma. An RF (13.56 MHz) power of 100 W is also supplied to the substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. In the second etching treatment, the Al–Ti film and the Ti film are etched selectively. Due to the second etching, the taper angle of the Al–Ti film and the Ti film became 80°. Due to the second etching treatment, a second conductive layer 19b and a third conductive layer 18b are formed. On the other hand, the first conductive layer 20a is hardly etched and a first conductive layer 20b is formed. Note that the second etching treatment herein corresponds to a second etching process (FIG. 1C) described in the above-mentioned embodiment mode. Accordingly, a second-shaped conductive layer was formed which is composed of the first conductive layer with a width of W1 in a channel length direction, the second conductive layer with a width of W2 therein, and the third conductive layer with a width of W3 therein. FIG. 2B shows an SEM photograph of the second-shaped conductive layer.

[0058]

Table 4 shows the results obtained by calculating a thickness (nm) of an underlying film to be etched, in the case where an etching rate of a film formed under the Al–Ti film with respect to the Al–Ti film is from 2 to 10, considering an in-plane variation of the etching rate of the Al–Ti film. At this time, the thickness was calculated assuming that the thickness of the Al–Ti film is 500 nm, and there is ±5% variation in a plane.

[0059]

[Table 4]

variation in an etching rate with respect to the Al–Ti film (±%)	selection ratio with respect to the underlying film								
	2	3	4	5	6	7	8	9	10
1	300.0	200.0	150.0	120.0	100.0	85.7	75.0	66.7	60.0
2	350.1	233.4	175.1	140.1	116.7	100.0	87.5	77.8	70.0
3	400.4	266.9	200.2	160.1	133.5	114.4	100.1	89.0	80.1
4	450.7	300.5	225.4	180.3	150.2	128.8	112.7	100.2	90.1
5	501.3	334.2	250.6	200.5	167.1	143.2	125.3	111.4	100.3
6	552.0	368.0	276.0	220.8	184.0	157.7	138.0	122.7	110.4
7	603.0	402.0	301.5	241.2	201.0	172.3	150.7	134.0	120.6
8	654.2	436.1	327.1	261.7	218.1	186.9	163.5	145.4	130.8
9	705.7	470.5	352.9	282.3	235.2	201.6	176.4	156.8	141.1
10	757.6	505.1	378.8	303.0	252.5	216.5	189.4	168.4	151.5
11	809.8	539.9	404.9	323.9	269.9	231.4	202.4	180.0	162.0
12	862.4	574.9	431.2	345.0	287.5	246.4	215.6	191.6	172.5
13	915.5	610.3	457.7	366.2	305.2	261.6	228.9	203.4	183.1
14	969.0	646.0	484.5	387.6	323.0	276.9	242.2	215.3	193.8
15	1023.0	682.0	511.5	409.2	341.0	292.3	255.8	227.3	204.6

[0060]

As shown in Table 4, the more increased the variation in an etching rate with respect to the Al–Ti film is, the larger the thickness to be etched becomes. Furthermore, the more a selection ratio with respect to the underlying film is increased, the thinner the thickness to be etched becomes. As these characteristics are utilized, a wiring with a desired shape can be formed.

[0061]

As described above, according to the present invention, since a gate line is formed of low-resistant conductive layers, even if the area of a pixel portion is enlarged, the pixel can be sufficiently driven.

[0062]

[Embodiment 2]

In the present embodiment, the case where the condition in the first etching condition in Embodiment 1 is changed will be described below. Herein, since the condition in the first etching condition is changed, only two layers (second and third conductive layers) in Embodiment 1 constitute a gate line. However, the present invention is also applicable to the case where a gate line is composed of three layers using the first conductive layer in Embodiment 1 as a lower layer.

[0063]

First, an oxynitride film 33 is formed to have a thickness of 200 nm on a 1737 glass substrate 10 by sputtering method. Then, a first conductive film 34 made of an Al–Ti film with a thickness of 500 nm and a second conductive film 35 made of a Ti film with a thickness of 100 nm were layered by sputtering method (FIG. 3A).

[0064]

Then, an etching treatment is conducted. This etching treatment corresponds to the first etching condition in Embodiment 1. In the present embodiment, an ICP (Inductively Coupled Plasma) etching method was used, and BCl_2 and Cl_2 were used as an etching gas under a pressure of 1.2 Pa. Etching was conducted by varying a gas flow rate and an electric power supplied to a coil-shaped electrode and a substrate side (sample stage) as shown in Table 5.

[0065]

[Table 5]

	ICP	Bias	gas	flow	etching time
condition	(W)	(W)		(sccm)	(s)
1	100	300	BCl3 / Cl2	60 / 20	268
2	300	300	BCl3 / Cl2	60 / 20	168
3	700	300	BCl3 / Cl2	60 / 20	159
4	500	100	BCl3 / Cl2	60 / 20	175
5	500	200	BCl3 / Cl2	60 / 20	147
6	500	400	BCl3 / Cl2	60 / 20	147

7	500	300	BCl3 / Cl2	20 / 60	60
8	500	300	BCl3 / Cl2	40 / 40	81
9	500	300	BCl3 / Cl2	70 / 10	350

[0066]

FIGs. from 4 to 6 show configurations of conductive layers obtained under the conditions shown in Table 5. It is understood from FIG. 4 that the more increased an electric power supplied to a coil-shaped electrode is, the larger a taper angle becomes. It is understood from FIG. 5 that the more increased an electric power supplied to a substrate side is, the larger a taper angle becomes. It is understood from FIG. 6 that the more increased a gas flow rate of BCl_2 is, the larger a taper angle becomes. Thus, it is understood that a taper angle is varied depending upon the condition. Furthermore, Table 6 shows etching rates obtained under the conditions shown in Table 5. Table 7 shows a selection ratio with respect to each film. Anisotropic etching is made possible under the condition that a selection ratio between Al–Ti and W is large, whereby a conductive layer with a desired shape can be formed.

[0067]

[Table 6]

	ICP	Bias	Gas flow	Al-Si (nm/min)		resist (nm/min)		W (nm/min)		SiON (nm/min)	
condition	(W)	(W)	(sccm)	(Ave)	(3σ)	(Ave)	(3σ)	(Ave)	(3σ)	(Ave)	(3σ)
1	100	300	60 / 20	168.8	39.3	122.4	33.1	37.1	6.4	38.4	8.1
2	300	300	60 / 20	236.9	51.4	197.9	36.7	59.4	16.2	66.4	8.9
3	700	300	60 / 20	262.1	63.2	263.1	33.2	110.7	23.1	107.6	12.0
4	500	100	60 / 20	236.7	40.6	133.7	26.3	41.4	17.0	56.0	8.2
5	500	200	60 / 20	246.8	46.1	199.6	23.7	69.1	22.3	81.8	8.8
6	500	400	60 / 20	251.0	55.2	255.3	24.4	102.6	21.3	104.0	13.4
7	500	300	20 / 60	750.7	111.0	395.2	70.7	127.8	49.9	104.0	17.6
8	500	300	40 / 40	495.6	116.5	351.1	62.2	112.4	39.4	101.0	16.8
9	500	300	70 / 10	142.3	24.2	148.6	17.7	61.0	10.8	99.3	9.7

[0068]

[Table 7]

condition	selection ratio with respect to Al-Si			selection ratio with respect to resist			selection ratio with respect to W			selection ratio with respect to SiON		
	resist	W	SiON	Al-Si	W	SiON	Al-Si	resist	SiON	Al-Si	resist	W
1	1.38	4.55	4.40	0.73	3.30	3.19	0.22	0.30	0.97	0.23	0.31	1.03
2	1.20	3.99	3.57	0.84	3.33	2.98	0.25	0.30	0.89	0.28	0.34	1.12
3	1.00	2.37	2.44	1.00	2.38	2.45	0.42	0.42	1.03	0.41	0.41	0.97
4	1.77	5.72	4.23	0.56	3.23	2.39	0.17	0.31	0.74	0.24	0.42	1.35
5	1.24	3.57	3.02	0.81	2.89	2.44	0.28	0.35	0.85	0.33	0.41	1.18
6	0.98	2.45	2.41	1.02	2.49	2.46	0.41	0.40	0.99	0.41	0.41	1.01
7	1.90	5.88	7.22	0.53	3.09	3.80	0.17	0.32	1.23	0.14	0.26	0.81
8	1.41	4.41	4.91	0.71	3.12	3.47	0.23	0.32	1.11	0.20	0.29	0.90
9	0.96	2.33	1.43	1.04	2.44	1.50	0.43	0.41	0.61	0.70	0.67	1.63

[0069]

As described above, by varying the condition, a conductive layer with a desired shape can be obtained. Furthermore, even if the area of a pixel portion is enlarged, a pixel can be sufficiently driven.

[0070]

[Embodiment 3]

In the present embodiment, the case where a plasma treatment is conducted to the wiring formed in Embodiment 1 will be described with reference to FIG. 17. Note that, in the present specification, a plasma treatment refers to a treatment exposing a sample to an atmosphere in which a gas is subjected to a plasma treatment.

[0071]

First, in accordance with Embodiment 1, the state shown in FIG. 1C is obtained. Note that FIG. 17A and FIG. 1C show the same state, and corresponding portions are denoted with the same reference numerals.

[0072]

The wiring thus formed is subjected to a plasma treatment using oxygen, a gas mainly containing oxygen, or H_2O (FIG. 17B). The plasma treatment is conducted for from 30 seconds to 20 minutes (preferably, from 3 to 15 minutes), using a plasma generating apparatus (plasma CVD apparatus, dry etching apparatus, sputtering apparatus, etc.). Furthermore, it is desirable that the wiring is treated under the condition of a gas flow rate of from 50 to 300 sccm, a substrate temperature of 200°C in room temperature, and an RF of from 100 to 2000 W. Due to the plasma treatment, Al or a second conductive layer composed of an alloy mainly containing Al or a conductive layer made of a compound is likely to be oxidized among the conductive layers constituting a three-layered structure. Therefore, a portion 22 that is not in contact with the other conductive layers is oxidized. This enables formation of projections such as hillock and whisker to be further reduced.

[0073]

Needless to say, when ashing is conducted using oxygen or a gas mainly containing oxygen, or H_2O in order to remove a resist 17b, the exposed portions of the second conductive layer are oxidized. However, a sufficient oxide film is more likely to be formed when a plasma treatment is conducted after removing the resist 17b.

[0074]

As described above, according to the present invention, a gate line is formed of low-resistant conductive layers. Therefore, even if the area of a pixel portion is enlarged, a pixel can be sufficiently driven.

[0075]

[Embodiment 4]

An example of manufacturing a wiring board by applying the present invention to a wiring structure different from those in Embodiments from 1 to 3 will be described with reference to FIG. 7.

[0076]

First, as a substrate 10, a glass substrate, a quartz substrate, a silicon substrate, or a substrate an insulating film is formed on a metal substrate or on a surface of a stainless steal substrate may be used. Furthermore, a plastic substrate may also be employed when it has a heat resistance against the process temperature. In the present embodiment, a glass substrate 1737 produced by Corning Co. is used.

[0077]

Then, a first conductive film 44 with a thickness of from 20 to 100 nm, a second conductive film 45 with a thickness of from 100 to 800 nm, and a third conductive film 46 with a thickness of from 20 to 100 nm are layered on the substrate 10. Herein, these conductive films may be formed using sputtering method, and as a first conductive layer contacting with the insulating film, a conductive film mainly containing W or Mo may be used so as to prevent diffusion of impurities from the substrate 10. Furthermore, as a second conductive layer, a low-resistant conductive film mainly containing Al or Cu may be used. As a third conductive layer, a conductive film mainly containing Ti with a low contact resistance may be used. In the present embodiment, these conductive films may be formed by sputtering method, and the first conductive film 44 made of an Mo film with a thickness of 30 nm, the second conductive film 45 made of an Al–Ti film with a thickness of 500 nm, and the third conductive film 46 made of a Ti film with a thickness of 50 nm are layered.

[0078]

Then, an etching treatment is conducted. The etching treatment is conducted under a first etching condition and a second etching condition. In the present embodiment, as the first etching condition, an ICP (Inductively Coupled Plasma) etching method was used. More specifically, etching was conducted, using BCl_2, Cl_2, and O_2 as an etching gas in a gas flow rate of 65/10/5 (sccm) with an RF (13.56 MHz) power of 450 W supplied to a coil-shaped electrode under a pressure of 1.2 Pa to generate plasma. Herein, a dry etching apparatus (Model E645–□ICP) using ICP produced by Matsushita Electric Industrial Co., Ltd. was used. An RF (13.56 MHz) power of 300 W is also supplied to a substrate side (sample stage),

whereby a substantially negative self-bias voltage is applied thereto. Under the first etching condition, the Al–Ti film and the Ti film are etched to taper the edges of the first conductive layer. Furthermore, under the first etching condition, although the taper angle of the Al–Ti film and the Ti film becomes about 45°, Mo is not etched.

[0079]

Thereafter, the etching condition is changed to the second etching condition without removing a resist mask 47. Under the second etching condition, etching was conducted, using CF_4, Cl_2, and O_2 as an etching gas in a gas flow rate of 25/25/10 (sccm) with an RF (13.56 MHz) power of 500 W supplied to a coil-shaped electrode under a pressure of 1 Pa to generate plasma. An RF (13.56 MHz) power of 20 W is also supplied to a substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. Under the second etching condition in which CF_4, Cl_2, and O_2 are mixed, only the Mo film is etched. Note that, in order to conduct etching without leaving a residue on a gate insulating film, it is preferable that an etching time may be increased by about from 10 to 20%.

[0080]

In the above-mentioned etching treatment, by making the shape of a resist mask appropriate, the edges of the first and second conductive layers are tapered due to the effect of a bias voltage applied to the substrate side. The taper angle may be set to be from 15° to 45°. Accordingly, a conductive layer composed of a first conductive layer 50, a second conductive layer 49, and a third conductive layer 48 is formed by the etching treatment.

[0081]

Then, an insulating film 51 is formed so as to cover the conductive layer. The insulating film 51 is formed using plasma CVD method or sputtering method to have a thickness of from 40 to 150 nm so as to have a single-layered structure or a multi-layered structure of an insulating film containing silicon. In the present embodiment, a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) is formed to have a thickness of 110 nm by plasma CVD method.

[0082]

Then, a semiconductor layer 52 is formed on the insulating film 51. The semiconductor layer 52 is obtained by forming a semiconductor film having an amorphous structure by a known method (sputtering method, LPCVD method, plasma CVD method, etc.), followed by patterning a crystalline semiconductor film obtained by conducting a known crystallization treatment (laser crystallization method, thermal crystallization method, thermal crystallization method using a catalyst such as nickel, etc.) into a desired shape using a photomask. The semiconductor layer 52 is formed to have a thickness of from 25 to 300 nm (preferably, from 30 to 150 nm). There is no particular limit to a material for the crystalline semiconductor film; however, the crystalline semiconductor film may be preferably formed of silicon, a silicon-germanium (SiGe) alloy, or the like. In the present embodiment, an amorphous silicon film is formed using plasma CVD method to have a thickness of 55 nm, and the amorphous silicon film is subjected to a laser annealing treatment to form a crystalline silicon film. The crystalline silicon film is patterned by photolithography method to form the semiconductor layer 42.

[0083]

As described above, according to the present invention, a gate line is formed of low-resistant conductive layers. Therefore, also in the case of using a TFT with a reverse-stagger structure, even if the area of a pixel portion is enlarged, a pixel can be sufficiently driven.

[0084]

[Embodiment 5]

In the present embodiment, as an exemplary wiring board utilizing the present invention, a method of manufacturing an active matrix substrate will be described with reference to FIGs. from 8 to 11. Note that, in the present specification, a substrate on which a driving circuit having a CMOS circuit and a pixel portion having a pixel TFT and a storage capacitor are formed on the same substrate will be referred to as an active matrix substrate for convenience.

[0085]

First, in the present embodiment, a substrate 400 made of glass such as barium borosilicate glass, typical example of #7059 glass or #1737 glass produced by Corning Co., or aluminoborosilicate glass is used. Note that, as the substrate 400, a quartz substrate, a silicon substrate, or a substrate an insulating film is formed on a metal substrate or on a surface of a stainless steal substrate may be also used. Furthermore, a plastic substrate may be also employed when it has a heat resistance against the process temperature of the present embodiment.

[0086]

Then, a base film 401 composed of an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed on the substrate 400. In the present embodiment, the base film 401 is formed from a double-layered structure; however, the base film 401 may be also formed from a single-layered film of said insulating film or a multi-layered structure of two or more layers. As a lower layer of the base film 401, a silicon oxynitride film 401a is formed to have a thickness of from 10 to 200 nm (preferably, from 50 to 100 nm) that SiH_4, NH_3, and N_2O are formed as a reaction gas, using plasma CVD method. In the present embodiment, the silicon oxynitride film 401a with a thickness of 50 nm (composition ratio: Si = 32%, O = 27%, N = 24%, H = 17%) was formed. Then, as an upper layer of the base film 401, a silicon oxynitride film 401b is formed to have a thickness of from 50 to 200 nm (preferably, from 100 to 150 nm) that SiH_4 and N_2O are formed as a reaction gas, using plasma CVD method. In the present embodiment, the silicon oxynitride film 401b with a thickness of 100 nm (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) is formed.

[0087]

Then, semiconductor layers from 402 to 406 are formed on the base film. The semiconductor layers from 402 to 406 are obtained by forming a semiconductor film to have a thickness of from 25 to 80 nm (preferably, from 30 to 60 nm) by a known method (sputtering method, LPCVD method, plasma CVD method, or the like), and by being subjected to crystallization by known crystallization (laser

crystallization method, thermal crystallization method using an annealing furnace or rapid thermal annealing (RTA)). The obtained crystalline semiconductor film is patterned into a desired shape to form the semiconductor layers from 402 to 406. As said semiconductor film, an amorphous semiconductor film, a microcrystalline semiconductor film, and a crystalline semiconductor film are included; however, a compound semiconductor film having an amorphous structure such as an amorphous silicon germanium film may be also used. In the present embodiment, an amorphous silicon film was formed to have a thickness of 55 nm, using plasma CVD method. A solution containing nickel was held on the amorphous silicon film and the amorphous silicon film was dehydrogenated at 500°C for an hour, and then, subjected to thermal crystallization at 550°C for 4 hours to form a crystalline silicon film. The crystalline silicon film was patterned by photolithography method to form semiconductor layers from 402 to 406.

[0088]

In the case of manufacturing a crystalline semiconductor film by laser crystallization method, YAG laser, YVO_4 laser, YLF laser, $YAlO_3$ laser, glass laser, ruby laser, alexandrite laser, Ti:sapphire laser, and the like of a continuous oscillation type or pulse oscillation type can be used. In the case of using these lasers, it is preferable to use a method that a laser beam emitted from a laser oscillator may be condensed into a linear shape by an optical system and radiated to a semiconductor film. The conditions for crystallization are appropriately selected by those skilled in the art. However, in the case of using excimer laser, a pulse oscillation frequency is set to be 300 Hz, and a laser energy density is set to be from 100 to 1200 mJ/cm^2 (typically, from 200 to 800 mJ/cm^2). Furthermore, in the case of using YAG laser, its second harmonics are used and a pulse oscillation frequency is set to be from 1 to 300 Hz, and a laser energy density is preferably set to be from 300 to 1200 mJ/cm^2 (typically, from 350 to 1000 mJ/cm^2). It may be also possible that laser light condensed into a linear shape with a width of from 100 to 1000 μm, for example 400 μm, is radiated over the entire surface of a substrate, and an overlap ratio of linear beams is set to be from 50 to 98%.

[0089]

However, in the present embodiment, an amorphous silicon film is crystallized using a metal element accelerating crystallization, so that said metal element remains in the crystalline silicon film. Therefore, an amorphous silicon film with a thickness of from 50 to 100 nm is formed on said crystalline silicon film, a heat treatment (thermal annealing using an annealing furnace, RTA, etc.) is conducted to diffuse said metal element into the amorphous silicon film, and said amorphous silicon film is removed by etching after the heat treatment. Because of this, the content of the metal element in said crystalline silicon film can be reduced or removed.

[0090]

In addition, after forming the semiconductor layers from 402 to 406, doping of a trace amount of impurity elements (boron or phosphorus) may be also conducted so as to control a threshold value of a TFT.

[0091]

Then, a gate insulating film 407 is formed so as to cover the semiconductor layers from 402 to 406. The gate insulating film 407 is formed of an insulating film containing silicon so as to have a thickness of from 40 to 150 nm using plasma CVD method or sputtering method. In the present embodiment, a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) was formed to have a thickness of 110 nm by plasma CVD method. It should be appreciated that the gate insulating film is not limited to a silicon oxynitride film, and may be also used as a single-layered structure or a multi-layered structure of another insulating film containing silicon.

[0092]

In the case of using a silicon oxide film, the silicon oxide film can be formed by plasma CVD method. More specifically, the silicon oxide film can be formed by mixing tetraethyl orthosilicate (TEOS) with O_2, setting a reaction pressure at 40 Pa and a substrate temperature at from 300°C to 400°C, and allowing discharge to be conducted at a high-frequency (13.56 MHz) electric density of from 0.5 to 0.8

W/cm^2. The silicon oxide film thus manufactured can obtain satisfactory electrical characteristics as a gate insulating film by thermal annealing at from 400°C to 500°C.

[0093]

Then, a first conductive film 408a with a thickness of from 20 to 100 nm, a second conductive film 408b with a thickness of from 100 to 800 nm, and a third conductive film 408c with a thickness of from 20 to 100 nm are layered on the gate insulating film 407. In the present embodiment, the first conductive film 408a made of a WN film with a thickness of 30 nm, the second conductive film 408b made of an Al–Sc film with a thickness of 370 nm, and the third conductive film 408c made of a TiN film with a thickness of 30 are layered.

[0094]

Note that in the present embodiment, although the first conductive film 408a was set to be WN, there is no particular limit thereto. As the first conductive film, a conductive layer made of an element selected from W and Mo, or an alloy or compound mainly containing said element, may be also formed. Furthermore, although the second conductive film 408b was set to be Al–Sc, there is no particular limit thereto. As the second conductive film, a conductive layer made of Al, or an alloy or compound mainly containing Al, may be also formed. Furthermore, although the third conductive film 408c was set to be TiN, there is no particular limit thereto. As the third conductive film, a conductive layer made of Ti, or an alloy or compound mainly containing Ti, may be also formed.

[0095]

Next, resist masks from 410 to 415 are formed using photolithography method, whereby a first etching treatment for forming electrodes and wiring is conducted. The first etching treatment is conducted under a first etching condition and a second etching condition (FIG. 8B). In the present embodiment, as the first etching condition, an ICP (Inductively Coupled Plasma) etching method is used. More specifically, etching is conducted, using BCl_2, Cl_2, and O_2 as an etching gas in a gas flow rate of 65/10/5 (sccm) with an RF (13.56 MHz) power of 450 W supplied

to a coil-shaped electrode under a pressure of 1.2 Pa to generate plasma. An RF (13.56 MHz) power of 300 W is also supplied to a substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. Under the first etching condition, the Al–Sc film and the TiN film are etched to taper the edges of the second and third conductive layers. Furthermore, under the first etching condition, although the taper angle of the Al–Sc film and the TiN film becomes about 45°, WN film is hardly etched.

[0096]

Thereafter, the etching condition is changed to the second etching condition without removing the resist masks from 410 to 415. Under the second etching condition, etching is conducted, using CF_4, Cl_2, and O_2 as an etching gas in a gas flow rate of 25/25/30 (sccm) and with an RF (13.56 MHz) power of 500 W supplied to a coil-shaped electrode under a pressure of 1 Pa to generate plasma. An RF (13.56 MHz) power of 20 W is also supplied to a substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. Note that, in order to conduct etching without leaving a residue on a gate insulating film, it is preferable that an etching time may be increased by about from 10 to 20%.

[0097]

In the above-mentioned first etching treatment, by making the shape of a resist mask appropriate, the edges of from the first to third conductive layers are tapered due to the effect of a bias voltage applied to the substrate side. The taper angle may be set to be from 15° to 45°. Accordingly, first-shaped conductive layers from 417 to 422 (first conductive layers from 417a to 422a, second conductive layers from 417b to 422b, and third conductive layers from 417c to 422c) composed of the first, second, and third conductive layers are formed by the first etching treatment. Reference numeral 416 denotes a gate insulating film. Regions of the gate insulating film 416 not covered with the first-shaped conductive layers from 417 to 422 are etched by about from 20 to 50 nm to form a thin region.

[0098]

Then, a second etching process is conducted without removing the resist

masks (FIG. 8C). Herein, etching was conducted, using BCl_3 and Cl_2 as an etching gas in a gas flow rate of 20/60(sccm) and with an RF (13.56 MHz) power of 600 W supplied to a coil-shaped electrode under a pressure of 1.2 Pa to generate plasma. An RF (13.56 MHz) power of 100 W is also supplied to the substrate side (sample stage), whereby a substantially negative self-bias voltage is applied thereto. In the second etching treatment, the Al–Sc film and the TiN film are selectively etched. At this time, due to the second etching treatment, second conductive layers from 428b to 433b and second conductive layers from 428c to 433c are formed. On the other hand, the first conductive layers from 417a to 422a are hardly etched, whereby second-shaped conductive layers from 428 to 433 are formed.

[0099]

As described above, due to a first etching process and a second etching process, gate electrodes from 428 to 431, an electrode 432 one of a storage capacitor, and a source line 433, using the constitution of the present invention, are formed.

[0100]

Then, a first doping treatment is conducted without removing the resist masks, whereby an impurity element imparting n-type is added to the semiconductor layers in a low concentration. The doping treatment may be conducted by ion doping method or ion implantation method. Ion doping method is conducted under the condition of a dose amount of from 1×10^{13} to $5 \times 10^{14}/cm^2$ and an acceleration voltage of from 40 to 80 keV. In the present embodiment, ion doping is conducted under the condition of a dose amount of $1.5 \times 10^{13}/cm^2$ and an acceleration voltage of 60 keV. As an impurity element imparting n-type, an element belonging to Group 15, typically, phosphorus (P) or arsenic (As), is used, and herein, phosphorus (P) is used. In this case, the conductive layers from 428 to 433 function as masks with respect to the impurity element imparting n-type, and impurity regions from 423 to 427 are formed in a self-alignment manner. An impurity element imparting n-type is added to the impurity regions from 423 to 427 so as to have a concentration range of from 1×10^{18} to $1 \times 10^{20}/cm^3$.

[0101]

After the resist masks are removed, resist masks from 434a to 434c are newly formed, and a second doping treatment is conducted at an acceleration voltage higher than that of the first doping treatment. Ion doping method at this time is conducted under the condition of a dose amount of from 1×10^{13} to $1 \times 10^{15}/cm^2$, and an acceleration voltage of from 60 to 120 keV. The doping treatment is conducted using the second conductive layers from 428b to 432b as masks with respect to an impurity element so that the impurity element is added to the semiconductor layers below the taper portions of the first conductive layers. Then, a third doping treatment is conducted at an acceleration voltage lower than that of the second doping treatment, whereby a state shown in FIG. 9A is obtained. At this time, ion doping method is conducted under the condition of a dose amount of from 1×10^{15} to $1 \times 10^{17}/cm^2$, and an acceleration voltage of from 50 to 100 keV. Due to the second and third doping treatment, an impurity element imparting n-type is added to low-concentration impurity regions 436, 442, and 448 overlapped with the first conductive layers in a concentration range of from 1×10^{18} to $5 \times 10^{19}/cm$. On the other hand, an impurity element imparting n-type is added to high-concentration impurity regions 435, 438, 441, 444, and 447 in a concentration range of from 1×10^{19} to $5 \times 10^{21}/cm^3$.

[0102]

Needless to say, by setting an appropriate acceleration voltage, the second and third doping treatments can be formed by one doping treatment, and the low-concentration impurity regions and the high-concentration impurity regions can be also formed.

[0103]

Then, after the resist masks are removed, resist masks from 450a to 450c are newly formed, and a fourth doping treatment is conducted. Due to the fourth doping treatment, impurity regions from 453 to 456, 459, and 460, in which an impurity element providing a conductivity type opposite to said one conductivity type is added, are formed in the semiconductor layers to be active layers of p-channel type TFTs. Second conductive layers from 428a to 432a are used as

masks with respect to an impurity element, and an impurity element imparting p-type is added, whereby impurity regions are formed in a self-alignment manner. In the present embodiment, the impurity regions from 453 to 456, 459, and 460 are formed by ion doping method using diborane (B_2H_6) (FIG. 9B). During the fourth doping treatment, the semiconductor layers constituting the n-channel type TFTs are covered with the resist masks from 450a to 450c. Due to from the first to third doping treatment, phosphorus is added to the impurity regions 438 and 439 in different concentrations. However, doping is conducted in both of the regions so that the concentration of an impurity element imparting p-type becomes from 1×10^{19} to 5×10^{21} atoms/cm^3, whereby these regions function as a source region and a drain region of a p-channel type TFT. Therefore, there is no problem.

[0104]

Due to the above-mentioned processes, impurity regions are formed in each semiconductor layer.

[0105]

Then, the resist masks from 450a to 450c are removed, and a first interlayer insulating film 461 is formed. The first interlayer insulating film 461 is made of an insulating film containing silicon with a thickness of from 100 to 200 nm, using plasma CVD method or sputtering method. In the present embodiment, a silicon oxynitride film with a thickness of 150 nm was formed by plasma CVD method. Needless to say, the first interlayer insulating film 461 is not limited to a silicon oxynitride film, and may be formed from a single-layered structure or a multi-layered structure of another insulating film containing silicon.

[0106]

Then, as shown in FIG. 9C, crystallinity of the semiconductor layers is recovered, and the impurity elements added to the respective semiconductor layers are activated by irradiation with a laser beam. In particular, laser annealing method using a YAG laser is preferred to be conducted. In the case where projections such as hillock and whisker are not formed even by a heat treatment due to regions contacting with the first interlayer insulating film in the second conductive layers

are sufficiently oxidized, thermal annealing method using an annealing furnace or Rapid Thermal Annealing method (RTA method) can be applied.

[0107]

A heat treatment may be conducted before forming the first interlayer insulating film. However, in the case where wiring to be used to heat is weak, it is preferable that an activation treatment is conducted after the interlayer insulating film (insulating film mainly containing silicon, e.g., silicon nitride film) is formed so as to protect wiring and the like as in the present embodiment.

[0108]

Then, hydrogenation can be conducted by a heat treatment (from 300°C to 450°C for from 1 to 12 hours). In this process, dangling bonds of the semiconductor layers are terminated due to hydrogen contained in the first interlayer insulating film 461. Irrespective of the presence of the first interlayer insulating film, the semiconductor layers can be hydrogenated. As an alternative method of hydrogenation, plasma hydrogenation (using hydrogen excited by plasma) or a heat treatment at from 300°C to 450°C for from 1 to 12 hours in an atmosphere containing from 3 to 100% hydrogen may be conducted.

[0109]

Next, a second interlayer insulating film 462a made of an inorganic insulating film material or an organic insulating material is formed on the first interlayer insulating film 461. In the present embodiment, an acrylic resin film with a thickness of 1.6 μm is formed, and that with a viscosity of from 10 to 1000 cp, preferably, from 40 to 200 cp, and that in which unevenness is formed on the surface is used. In the case where an organic resin film is not used, a second interlayer insulating film 462b with a shape as shown in FIG. 21 is formed.

[0110]

In the present embodiment, in order to prevent mirror reflection, the second interlayer insulating film, on which unevenness is provided, is formed, whereby unevenness was formed on the surface of pixel electrodes. Furthermore, in order to obtain light scattering by forming unevenness on the surface of pixel electrodes,

convex portions may be formed in lower regions of the pixel electrodes. In that case, the convex portions can be formed by using the same photomask as that for forming a TFT. Therefore, the convex portions can be formed without increasing the number of processes. The convex portions may be appropriately provided on the substrate in the pixel portion region besides and a TFT portion. Accordingly, unevenness is formed on the surface of pixel electrodes along the unevenness formed on the surface of the insulating film covering the convex portions.

[0111]

As the second interlayer insulating film 462a, a film whose surface is to be flattened may be also used. In that case, it is preferable that, after pixel electrodes are formed, the surface is provided with unevenness by adding the processes of known sand blast method, etching method, and the like to prevent mirror reflection and allow reflected light to scatter, thereby enhancing whiteness.

[0112]

Furthermore, in a driving circuit 506, wires from 464 to 468 electrically connected to the respective impurity regions are formed. Note that, these wires are formed by patterning a layered film of a Ti film with a thickness of 50 nm and an alloy film (alloy film of Al and Ti) with a thickness of 500 nm. It should be appreciated that the wires are not limited to a double-layered structure and may have a single-layered structure or a multi-layered structure of three or more layers. Furthermore, a material for wiring is not limited to Al and Ti. For example, a layered film obtained by forming Al or Cu on a TaN film and forming a Ti film thereon may be patterned to form wiring (FIG. 10).

[0113]

In a pixel portion 507, a pixel electrode 470, a gate line 469, and a connection electrode 468 are formed. Due to the connection electrode 468, a source line (layer of 443a and 443b) is electrically connected to a pixel TFT. Furthermore, the gate line 469 is electrically connected to a gate electrode of a pixel TFT. Furthermore, the pixel electrode 470 is electrically connected to a drain region 442 of a pixel TFT, and electrically connected to the semiconductor layer 458 that functions as one

electrode constituting a storage capacitor. As the pixel electrode 471, a material excellent in reflectivity such as a film mainly containing Al or Ag, or a layered film thereof is desired to be used.

[0114]

As described above, the driving circuit 506 having a CMOS circuit composed of an n-channel type TFT 501 and a p-channel type TFT 502, and an n-channel type TFT 503, and the pixel portion 507 having a pixel TFT 504 and a storage capacitor 505 can be formed on the same substrate. Thus, an active matrix substrate is completed.

[0115]

The n-channel type TFT 501 of the driving circuit 506 has a channel-formation region 437, the low-concentration impurity region 436 (GOLD region) overlapped with the first conductive layer 428a constituting a part of a gate electrode, a high-concentration impurity region 452 that function as a source region or a drain region, and an impurity region 451 in which an impurity element imparting n-type and an impurity element imparting p-type are introduced. The n-channel type TFT 501 and the p-channel type TFT 502 electrically connected to the electrode 466 and constituting a CMOS circuit have a channel-formation region 440, the high-concentration impurity region 454 that function as a source region or a drain region, and the impurity region 453 in which an impurity element imparting n-type and an impurity element imparting p-type are introduced. Furthermore, the n-channel type TFT 503 has a channel-formation region 443, the low-concentration impurity region 442 (GOLD region) overlapped with the first conductive layer 430a constituting a part of a gate electrode, and the high-concentration impurity region 456 that function as a source region or a drain region, and the impurity region 455 in which an impurity element imparting n-type and an impurity element imparting p-type are introduced.

[0116]

The pixel TFT 504 of the pixel portion has a channel-formation regions 446, a low-concentration impurity region 445 (lightly doped drain (LDD) region) formed

outside of a gate electrode, a high-concentration impurity region 458 that function as a source region or a drain region, and an impurity region 457 in which an impurity element imparting n-type and an impurity element imparting p-type are introduced. Furthermore, an impurity element imparting n-type and an impurity element imparting p-type are added to the semiconductor layer that functions as one electrode of the storage capacitor 505. The storage capacitor 505 is composed of an electrode (layered structure of 432a and 432b) and the semiconductor layer using the insulating film 416 as a dielectric.

[0117]

In the pixel configuration of the present embodiment, the edges of the pixel electrode are disposed so as to be overlapped with a source line such that a gap between pixel electrodes is light-shielded without using a black matrix.

[0118]

Furthermore, FIG. 11 shows a top view of a pixel portion of an active matrix substrate manufactured in the present embodiment. Corresponding portions in FIGs. from 8 to 11 are denoted with the same reference numerals. A broken line A–A' in FIG. 10 corresponds to a cross-section taken along a broken line A–A' in FIG. 11. A broken line B–B' in FIG. 10 corresponds to a cross-section taken along a broken line B-B' in FIG. 11.

[0119]

In the wiring thus produced, low resistance is realized, and a wiring board having the wiring is fully designed for an enlarged pixel portion.

[0120]

The present embodiment can be arbitrarily combined with either of Embodiments from 1 to 4.

[0121]

[Embodiment 6]

In the present embodiment, the processes of manufacturing a reflection type liquid crystal display device using the active matrix substrate manufactured in Embodiment 5 will be described below with reference to FIG. 12.

[0122]

First, in accordance with Embodiment 5, the active matrix substrate as shown in FIG. 10 is obtained. Thereafter, an alignment film 567 is formed on the active matrix substrate in FIG. 10, at least on a pixel electrode 470, and a rubbing treatment is conducted. Note that in the present embodiment, before forming the alignment film 567, an organic resin film such as an acrylic resin film was patterned, whereby a column-shaped spacer 572 for holding a substrate gap was formed at a desired position. Furthermore, spherical spacers may be also scattered over the entire surface of the substrate, in place of column-shaped spacers.

[0123]

Then, a counter substrate 569 is prepared. Coloring layers 570 and 571, and a leveling film 573 are formed on the counter substrate 569. The red coloring layer 570 is overlapped with the blue coloring layer 571 to form a light-shielding portion. It may also be possible that a red coloring layer is partially overlapped with a green coloring layer to form a light-shielding portion.

[0124]

In the present embodiment, the substrate described in Embodiment 5 is used. Therefore, in FIG. 11 showing a top view of the pixel portion in Embodiment 5, it is required that at least the gap between a gate line 469 and the pixel electrode 470, the gap between the gate line 469 and a connection electrode 468, and the gap between the connection electrode 468 and the pixel electrode 470 should be light-shielded. In the present embodiment, each coloring layer was disposed so that a light-shielding portion composed of a stack of coloring layers was overlapped with positions to be light-shielded, under the condition that the counter substrate was attached.

[0125]

As described above, the gap between the respective pixels is light-shielded with a light-shielding portion composed of a stack of coloring layers, whereby the number of processes can be reduced, without forming a light-shielding layer such as a black mask.

[0126]

Then, a counter electrode 576 composed of a transparent conductive film was formed on the leveling film 573 at least in the pixel portion, and an alignment film 574 was formed over the entire surface of the counter substrate, whereby a rubbing treatment was conducted.

[0127]

Then, the active matrix substrate on which the pixel portion and the driving circuit are formed and the counter substrate are attached to each other with a sealant 568. Filler is mixed in the sealant 568, and two substrates are attached to each other at a uniform interval with the filler and column spacers. Thereafter, a liquid crystal material 575 is injected between the substrates, and the substrates are completely sealed with a sealant (not shown). A known liquid crystal material may be used for the liquid crystal material 575. Thus, a reflection type liquid crystal display device shown in FIG. 12 is completed. If required, the active matrix substrate or the counter substrate is separated in a desired shape. Furthermore, a polarizing plate (not shown) was attached only to the counter substrate. Then, a flexible printed circuit (FPC) was attached using a known technique.

[0128]

A liquid crystal display panel manufactured as described above can be used as a display portion of various electronic equipment. Said liquid crystal display panel is fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0129]

Note that, the present embodiment can be arbitrarily combined with either of Embodiments from 1 to 5.

[0130]

[Embodiment 7]

In the present embodiment, the processes of manufacturing an active matrix type liquid crystal display device different from that of Embodiment 7 from the active matrix substrate manufactured in Embodiment 6 will be described below with

reference to FIG. 11.

[0131]

First, in accordance with Embodiment 6, the active matrix substrate as shown in FIG. 8 is obtained. Thereafter, an alignment film 1067 is formed on the active matrix substrate in FIG. 8, and a rubbing treatment is conducted. Note that, in the present embodiment, before forming the alignment film 1067, an organic resin film such as an acrylic resin film was patterned, whereby a column-shaped spacer 572 for holding a substrate gap was formed at a desired position. Furthermore, spherical spacers may be also scattered over the entire surface of the substrate, in place of column-shaped spacers.

[0132]

Then, a counter substrate 1068 is prepared. The counter substrate is provided with a color filter in which a coloring layer 1074 and a light-shielding layer 1075 are disposed so as to correspond to each pixel. A light-shielding layer 1077 was also formed in a portion of a driving circuit. A leveling film 1076 covering the color filter and the light-shielding layer 1077 was provided. Then, a counter electrode 1069 made of a transparent conductive film on the leveling film 1076 was formed in the pixel portion, and an alignment film 1070 was formed over the entire surface of the counter substrate, followed by conducting a rubbing treatment.

[0133]

Then, the active matrix substrate on which the pixel portion and the driving circuit are formed and the counter substrate are attached to each other with a sealant 1071. Filler is mixed in the sealant 1071, and two substrates are attached to each other at a uniform interval with the filler and column spacers. Thereafter, a liquid crystal material 1073 is injected between the substrates, and the substrates are completely sealed with a sealant (not shown). A known liquid crystal material may be used for the liquid crystal material 1073. Thus, an active matrix type liquid crystal display device shown in FIG. 11 is completed. If required, the active matrix substrate or the counter substrate is separated in a desired shape. Furthermore, a

polarizing plate or the like was appropriately provided by using a known technique. Then, an FPC was attached by a known technique.

[0134]

A liquid crystal display panel manufactured as described above can be used as a display portion of various electronic equipment. Said liquid crystal display panel is fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0135]

Note that, the present embodiment can be arbitrarily combined with either of Embodiments from 1 to 5.

[0136]

[Embodiment 8]

In the present embodiment, as an example of a wiring board utilizing the present invention, exemplary production of a light-emitting device will be described. In the present specification, a light-emitting device collectively refers to a display panel in which a light-emitting element formed on a substrate is sealed between the substrate and cover member, and a display module in which an IC is mounted on the display panel. Note that, a light-emitting element has a layer (light-emitting layer) containing an organic compound that allows electroluminescence generated by application of an electric field, an anode layer, and a cathode layer. Furthermore, luminescence in an organic compound includes a light emitting (fluorescence) obtained when a singlet excited state returns to a normal state and a light emitting (phosphorescence) obtained when a triplet excited state returns to a normal state. Either one of or both of light emitting is included.

[0137]

FIG. 14 is a cross-sectional view of a light-emitting device of the present embodiment. In FIG. 14, a switching TFT 603 provided on a substrate 700 is formed by using an n-channel type TFT 503 in FIG. 10. Therefore, the description of the configuration may be referred to that of the n-channel type TFT 503.

[0138]

Although the present embodiment shows a double-gate structure in which two channel-formation regions are formed, a single-gate structure in which one channel-formation region is formed or a triple-gate structure in which three channel-formation regions are formed may be also used.

[0139]

A driving circuit provided on the substrate 700 is formed by using the CMOS circuit shown in FIG. 10. Therefore, regarding the description of the configuration of the driving circuit, the description of an n-channel type TFT 501 and a p-channel type TFT 502 may be referred to. Although the present embodiment shows a single-gate structure, a double-gate structure or a triple-gate structure may be also used.

[0140]

Furthermore, wires 701 and 703 function as source lines of a CMOS circuit, and a wire 702 functions as a drain line. A wire 704 functions as a wire for electrically connecting a source line 708 to a source region of a switching TFT, and a wire 705 functions as a wire electrically connecting a drain line 709 to a drain region of a switching TFT.

[0141]

A current control TFT 604 is formed by using the p-channel type TFT 502 in FIG. 10. Therefore, regarding the description of the current control TFT 604, the description of the p-channel TFT type 502 may be referred to. Although the present embodiment shows a single-gate structure, a double-gate substrate or a triple-gate structure may be also used.

[0142]

A wire 706 is a source line (corresponding to a current supply line) of the current control TFT, and reference numeral 707 denotes an electrode that is electrically connected to a pixel electrode 710 by being overlapped with the pixel electrode 710 of the current control TFT.

[0143]

Note that, the pixel electrode 710 is pixel electrode (an anode of a

light-emitting element) made of a transparent conductive film. As the transparent conductive film, a compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, or indium oxide can be used. Said transparent conductive film with gallium added thereto may be also used. The pixel electrode 710 is formed on a flat interlayer insulating film 711 before forming the above-mentioned wiring. In the present embodiment, it is very important to flatten the step difference caused by TFTs using a leveling film 711 made of a resin. A light-emitting layer to be formed later is very thin, so that light-emission defects may be caused due to the presence of the step difference. Therefore, it is desirable that the surface is flattened before forming pixel electrodes so that the light-emitting layer can be formed on a flat surface.

[0144]

After the wires from 701 to 707 are formed, a bank 712 is formed as shown in FIG. 14. The bank 712 may be formed by patterning an insulating film or an organic resin film, containing silicon with a thickness of from 100 to 400 nm.

[0145]

Since the bank 712 is made of an insulating film, care should be taken to electrostatic breakdown of element during film formation. In the present embodiment, a resistance is decreased by adding carbon particles or metal particles to an insulating film to be a material for the bank 712, whereby static electricity is suppressed. At this time, the adding amount of carbon particles or metal particles may be regulated so that a resistance becomes from 1×10^6 to 1×10^{12} Ωm (preferably, from 1×10^8 to 1×10^{10} Ωm).

[0146]

A light-emitting layer 713 is formed on the pixel electrode 710. Although only one pixel is shown in FIG. 14, light-emitting layers are formed so as to correspond to R (red), G (green), and B (blue) in the present embodiment. Furthermore, in the present embodiment, a low molecular-weight organic light-emitting material is formed by vapor deposition method. More specifically, a layered structure is used in which copper phthalocyanine (CuPc) film with a

thickness of 20 nm is provided as a hole injection layer, and a tris-8-quinolinolatoaluminum complex (Alq_3) film with a thickness of 70 nm is provided as a light-emitting layer on the hole injection layer. By adding fluorochrome such as quinacridon, perylene, or DCMl to Alq_3, a light-emission color can be controlled.

[0147]

It should be noted that above-mentioned example is an exemplary organic light-emitting material that can be used as a light-emitting layer, but the present embodiment is not necessarily limited thereto. A light-emitting layer (layer for light-emitting and moving carriers for light-emitting) may be formed by arbitrarily combining a light-emitting layer, a charge transport layer, or a charge injection layer. In the present embodiment, for example, a low molecular-weight organic light-emitting material used as a light-emitting layer was exemplified; however, a high molecular-weight organic light-emitting material may be also used. Furthermore, it is also possible to use an inorganic material such as silicon carbide as a charge transfer layer or a charge injection layer. As the organic light-emitting material and inorganic material, known materials can be used.

[0148]

Next, a cathode 714 made of a conductive film is provided on the light-emitting layer 713. In the present embodiment, an alloy film of aluminum and lithium is used as a conductive film. Needless to say, a known MgAg film (alloy film of magnesium and silver) may be also used. As a material for a cathode, a conductive film made of an element belonging to Group 1 or 2 of the periodic table, or a conductive film with these elements added thereto may be used.

[0149]

As of the cathode 714 is formed, a light-emitting element 715 is completed. Note that, the light-emitting element 715 herein refers to a diode formed of the pixel electrode (anode) 710, the light-emitting layer 713, and the cathode 714.

[0150]

It is effective that a passivation film 716 is provided so as to cover the

light-emitting element 715 completely. As the passivation film 716, a single-layered structure or a multi-layered structure of an insulating film including a carbon film, a silicon nitride film, or a silicon oxynitride film is used.

[0151]

In this case, a film with satisfactory coverage is preferably used as the passivation film. It is effective to use a carbon film, particularly, DLC film (diamond-like carbon). Since the DLC film can be formed in a temperature range from room temperature to 100°C or less, the DLC film can be easily formed even above the light-emitting layer 713 with low heat resistance. Furthermore, due to a high blocking effect with respect to oxygen, the DLC film can suppress oxidation of the light-emitting layer 713. Therefore, the light-emitting layer 713 can be prevented from being oxidized while the subsequent sealing process is conducted.

[0152]

Furthermore, a sealant 717 is provided on the passivation film 716, and a cover member 718 is attached to the sealant 717. As the sealant 717, a UV-curable resin may be used, and it is effective to provide a material having moisture-absorption effect or a material having an antioxidant effect. Furthermore, in the present embodiment, as the cover member 718, a glass substrate, a quartz substrate, or a plastic substrate (including a plastic film) with a carbon film (preferably, a diamond-like carbon film) formed on both sides thereof is used.

[0153]

Accordingly, a light-emitting device having a configuration as shown in FIG. 14 is completed. It is effective that up to the process the passivation film 716 is formed after the bank 712 is formed is continuously conducted without being exposed to the atmosphere using a film-formation apparatus of a multi-chamber type (or an in-line type). It is also possible that up to the process attached the cover member 718 is conducted continuously without being exposed to the atmosphere.

[0154]

Accordingly, n-channel type TFTs 601 and 602, the switching TFT (n-channel type TFT) 603, and the current control TFT (n-channel type TFT) 604 are formed on

the substrate 700.

[0155]

Furthermore, as described with reference to FIG. 14, by providing impurity regions overlapped with a gate electrode via an insulating film, an n-channel TFT that is unlikely to be degraded due to a hot-carrier effect can be formed. Therefore, a highly reliable light-emitting device can be realized.

[0156]

In the present embodiment, only the configurations of a pixel portion and a driving circuit are shown. However, in accordance with the manufacturing processes of the present embodiment, logic circuits such as a signal division circuit, a D/A converter, an operational amplifier, and a γ-correction circuit can be formed on the same insulator. Furthermore, even a memory and a microprocessor can be also formed.

[0157]

The light-emitting device of the present embodiment after up to the sealing (or encapsulation) process for protecting a light-emitting element is conducted will be described with reference to FIG. 15. If required, reference numerals used in FIG. 14 will be cited.

[0158]

FIG. 15A is a top view showing a state in which up to sealing of a light-emitting element is completed. FIG. 15B is a cross-sectional view taken along a line C–C' in FIG. 15A. Portions surrounded by dotted lines and denoted with reference numerals 801, 806, and 807 are a source-side driving circuit, a pixel portion, and a gate-side driving circuit, respectively. Reference numeral 901 denotes a cover member, 902 denotes a first sealant, 903 denotes a second sealant, and a sealing material 907 is provided in an inner portion surrounded by the sealant 902.

[0159]

Reference numeral 904 denotes a wiring for transmitting a signal input to the source-side driving circuit 801 and the gate-side driving circuit 807 and a video

signal and a clock signal are received from a flexible printed circuit (FPC) 905 to be an external input terminal. Herein, although only an FPC is shown, a printed wiring board (PWB) may be also attached to the FPC. The light-emitting device in the present specification includes not only a light-emitting device itself but also a state that a light-emitting device is attached to an FPC or a PWB.

[0160]

Next, a cross-sectional configuration will be described with reference to FIG. 15B. The pixel portion 806 and the gate-side driving circuit 807 are formed above the substrate 700. The pixel portion 806 is composed of a current control TFT 604 and a plurality of pixels including a pixel electrode 710 electrically connected to a drain of the current control TFT 604. Furthermore, the gate-side driving circuit 807 is composed of a CMOS circuit (see FIG. 14) obtained by combining the n-channel type TFT 601 with the p-channel type TFT 602.

[0161]

The pixel electrode 710 functions as an anode of a light-emitting element. The bank 712 is formed at both ends of the pixel electrode 710, and the light-emitting layer 713 and the cathode 714 of a light-emitting element are formed over the pixel electrode 710.

[0162]

The cathode 714 also functions as wiring common to all the pixels, and is electrically connected to the FPC 905 via the connection line 904. Furthermore, all the elements contained in the pixel portion 806 and the gate-side driving circuit 807 are covered with the cathode 714 and the passivation film 567.

[0163]

The cover member 901 is attached with the first sealant 902. Note that, spacers made of a resin film may be also provided so as to ensure a gap between the cover member 901 and the light-emitting element. An inner portion of the first sealant 902 is filled with the sealant material 907. An epoxy resin is preferably used for the first sealant 902 and the sealant material 907. It is desirable that the first sealant 902 is to be a material unlikely to transmit moisture and oxygen as

possible. Furthermore, the sealing material 907 may also contain inside a material having moisture-absorption effect and an antioxidant effect.

[0164]

The sealing material 907 provided so as to cover the light-emitting element also functions as an adhesive for attaching the cover member 901. In the present embodiment, as a material for a plastic substrate 901a constituting the cover member 901, fiberglass-reinforced plastics (FRP), polyvinyl fluoride (PVF), Mylar, polyester, or acrylic resin can be used.

[0165]

Furthermore, after the cover member 901 is attached with the sealing material 907, the second sealant 903 is provided so as to cover the side surfaces (exposed surfaces) of the sealing material 907. The second sealant 903 can be made of the same material as that of the first sealant 902.

[0166]

By sealing the light-emitting element with the sealing material 907 in the above-mentioned configuration, the light-emitting element can be completely shut off from the outside, whereby a material accelerating degradation of the light-emitting layer due to oxidation, such as moisture and oxygen, can be prevented from entering from the outside. Thus, a highly reliable light-emitting device can be obtained. Furthermore, said light-emitting device can be fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0167]

Note that, the present embodiment can be arbitrarily combined with either of Embodiments from 1 to 5.

[0168]

[Embodiment 9]

In the present embodiment, a light-emitting device having a pixel configuration different from that in Embodiment 8 will be described with reference to FIG. 16.

[0169]

In FIG. 16, as a current control TFT 4501, a TFT having the same configuration as that of a p-channel TFT 502 in FIG. 10 is used, and as a switching TFT 4402, a TFT having the same configuration as that of a pixel TFT 504 in FIG. 10 is used. Needless to say, a gate electrode of the current control TFT 4501 is electrically connected to a drain line of the switching TFT 4402. Furthermore, a drain line of the current control TFT is electrically connected to a pixel electrode 4504.

[0170]

In the present embodiment, the pixel electrode 4504 made of a conductive film functions as a cathode of a light-emitting element. More specifically, an alloy film of aluminum and lithium is used. A conductive film made of an element belonging to Group 1 or Group 2 in the periodic table or a conductive film with the element added thereto may be used.

[0171]

A light-emitting layer 4505 is formed on the pixel electrode 4504. Note that, only one pixel is shown in FIG. 16, and in the present embodiment, a light-emitting layer corresponding to G (green) is formed by vapor deposition method and coating method (preferably, spin coating method). More specifically, the light-emitting layer has a multi-layered structure in which a lithium fluoride (LiF) film with a thickness of 20 nm is provided as an electron injection layer, and a polyparaphenylene vinylene (PPV) film with a thickness of 70 nm is provided thereon as a light-emitting layer.

[0172]

An anode 4506 made of a transparent conductive film is provided on the light-emitting layer 4505. In the present embodiment, as the transparent conductive film, a conductive film made of a compound of indium oxide and tin oxide or a compound of indium oxide and zinc oxide is used.

[0173]

As of the anode 4506 is formed, a light-emitting element 4507 is completed. The light-emitting element 4507 herein refers to a diode formed of the pixel

electrode (cathode) 4504, the light-emitting layer 4505, and the anode 4506.

[0174]

It is effective to provide a passivation film 4508 so as to cover the light-emitting element 4507 completely. As the passivation film 4508, a single-layered structure or a multi-layered structure of an insulating film including a carbon film, a silicon nitride film, or a silicon oxynitride film is used.

[0175]

Furthermore, a sealing material 4509 is provided on the passivation film 4508, and a cover member 4510 is attached to. As the sealing material 4509, UV-curable resin may be used, and it is effective to provide a material having moisture-absorption effect or an antioxidant effect in the sealing material 4509. In the present embodiment, as the cover member 4510, a glass substrate, a quartz substrate, or a plastic substrate (including a plastic film) with a carbon film (preferably, a diamond-like carbon film) formed on both sides thereof is used.

[0176]

In the wiring of the light-emitting device thus manufactured, low resistance is realized, and such a light-emitting device is fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0177]

Note that the present embodiment can be arbitrarily combined with either of Embodiments from 1 to 5.

[0178]

[Embodiment 10]

In the present embodiment, an exemplary liquid crystal display device using the present invention will be described in which a TFT configuration is different from that of an active matrix substrate manufactured in Embodiment 5.

[0179]

On an active matrix substrate shown in FIG. 18A, a driving circuit 506 having an n-channel type TFT 503 and a p-channel type TFT 502, and a pixel portion 507 having a pixel TFT 504 and a storage capacitor 505 are formed.

[0180]

These TFTs are obtained by forming gate lines from 512 to 517 on a substrate 510, forming an insulating film 511 on said gate lines, and providing channel-formation regions, source regions, drain regions, LDD regions, and the like in a semiconductor layer on said insulating film. The semiconductor layer is formed using the present invention in the same way as in Embodiments from 1 to 5.

[0181]

The gate lines from 512 to 517 are formed to have a thickness of from 200 to 400 nm, preferably, 250 nm, so that the edges of the gate lines from 512 to 517 are tapered so as to enhance step coverage of a coating film to be formed on upper layers thereof. The gate lines from 512 to 517 are formed so that the taper angle becomes from 5° to 30°, preferably, from 15° to 25°. The taper portions are formed by dry etching method, and the angle thereof is controlled with an etching gas and a bias voltage applied to the substrate side.

[0182]

Furthermore, impurity regions are formed in from first to third doping processes. First, the first doping process is conducted, whereby an LDD region of an n-channel type TFT is formed. Doping may be conducted by ion doping method or ion implantation method. Phosphorus (P) is added as an impurity element imparting n-type (donor), and first impurity regions from 219 to 222 are formed with a mask. Then, a mask is newly formed so as to cover the LDD region of the n-channel type TFT, whereby a source region and a drain region of the n-channel type TFT are formed during the second doping process.

[0183]

In the third doping treatment, a source region and a drain region of a p-channel type TFT are formed. Doping may be conducted by adding an impurity element imparting p-type (acceptor) by ion doping method or ion implantation method. At this time, the semiconductor layer in which an n-channel type TFT is to be formed is covered with a mask; therefore, the impurity element imparting p-type will not be added to the semiconductor layer. In the present embodiment,

although an LDD region is not manufactured in the p-channel type TFT, the LDD region may be also provided.

[0184]

Thus, in the n-channel type TFT 503, a LDD region 530 and a source region or a drain region 531 are formed outside of a channel-formation region 529. The p-channel type TFT 502 also has the same configuration and is composed of a channel-formation region 527, and a source region or a drain region 528. In the present embodiment, a single-gate structure is used; however, a double-gate structure or a triple-gate structure may be also used.

[0185]

In the pixel portion 507, the pixel TFT 504 formed of an n-channel type TFT has a multi-gate structure for the purpose of reducing an OFF-current, and an LDD region 533, and a source region or a drain region 534 are provided outside of a channel-formation region 532.

[0186]

An interlayer insulating film is composed of a first interlayer insulating film 540 with a thickness of from 50 to 500 nm made of an inorganic material such as silicon oxide, silicon nitride, or silicon oxynitride, and a second interlayer insulating film 541 made of an organic insulating material such as polyimide, acrylic resin, polyimideamide, and benzocyclobutene (BCB). Thus, by forming the second interlayer insulating film of an organic insulating material, the surface of the interlayer insulating film can be satisfactorily flattened. An organic resin material generally has a low dielectric constant; therefore, parasitic capacitance can be reduced. However, the organic resin material is not suitable as a protective film due to its moisture absorbency; therefore, it is preferable to combine with the first interlayer insulator 540.

[0187]

Thereafter, a resist mask with a predetermined pattern is formed, and contact holes reaching a source region or a drain region formed in each semiconductor layer are formed. The contact holes are formed by dry etching method. In this case,

the second interlayer insulating film 541 made of an organic resin material is first etched using a mixed gas of CF_4, O_2, and He as an etching gas, and thereafter, the first interlayer insulating film 540 is etched using CF_4 and O_2 as an etching gas.

[0188]

Then, a conductive metal film is formed by sputtering method or vacuum vapor evaporation method. A resist mask pattern is formed, and wires from 543 to 549 are formed by etching. Thus, an active matrix substrate can be formed.

[0189]

The process of manufacturing an active matrix type liquid crystal display device using the active matrix substrate in FIG. 18A will be described. FIG. 18B shows a state in which the active matrix substrate is attached to a counter substrate 554 with a sealant 558. First, column-shaped spacers 551 and 552 are formed on the active matrix substrate shown in FIG. 18A. The spacers 551 provided in the pixel portion are formed so as to be overlapped with a contact portion on the pixel electrode. Although a spacer depends upon a liquid crystal material to be used, the height of the spacers is set to be from 3 to 10 μm. In the contact portion, concave portions are formed corresponding to the contact holes. Therefore, by forming the spacers so that they are aligned with the concave portions, orientation of liquid crystal can be prevented from being disturbed. Thereafter, an alignment film 553 is formed, and a rubbing treatment is conducted. A transparent conductive film 555 and an alignment film 556 are formed on the counter substrate 554. Then, the active matrix substrate and the counter substrate are attached to each other, and liquid crystal is injected therebetween.

[0190]

An active matrix type liquid crystal display device manufactured as described above can be used as a display apparatus for various electronic devices. Said liquid crystal display panel is fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0191]

Note that, the present embodiment can be arbitrarily combined with either of

Embodiments from 1 to 5.

[0192]

[Embodiment 11]

In the present embodiment, the case will be described in which a light-emitting device is manufactured using an active matrix substrate described in Embodiment 10.

[0193]

In FIG. 19, as a current control TFT 4501, a TFT having the same configuration as that of an n-channel type TFT 503 in FIG. 16 is used. Needless to say, a gate electrode of the current control TFT 4501 is electrically connected to a drain line of a switching TFT 4402. A drain line of the current control TFT 4501 is electrically connected to a pixel electrode 4504.

[0194]

In the present embodiment, the pixel electrode 4504 made of a conductive film functions as a cathode of a light-emitting element. More specifically, an alloy film of aluminum and lithium is used. A conductive film made of an element belonging to Group 1 or 2 in the periodic table, or a conductive film with the element added thereto may be used.

[0195]

A light-emitting layer 4505 is formed on the pixel electrode 4504. Note that, in FIG. 19, only one pixel is shown, and in the present embodiment, a light-emitting layer corresponding to G (green) is formed by vapor deposition method and coating method (preferably, spin coating method). More specifically, a layered structure is used, in which a lithium fluoride (LiF) film with a thickness of 20 nm is provided as an electron injection layer, and a PPV (polyparaphenylene vinylene) film with a thickness of 70 nm is provided thereon as a light-emitting layer.

[0196]

Next, an anode 4506 made of a transparent conductive film is provided on the light-emitting layer 4505. In the present embodiment, a conductive film made of a compound of indium oxide and tin oxide, or a compound of indium oxide and zinc

oxide is used as a transparent conductive film.

[0197]

As of the anode 4506 is formed, a light-emitting element 4507 is completed. The light-emitting element 4507 refers to a diode composed of the pixel electrode (cathode) 4504, the light-emitting layer 4505, and the anode 4506.

[0198]

It is effective that a passivation film 4508 is provided so as to cover the light-emitting element 4507 completely. As the passivation film 4508, a single-layered structure or a multi-layered structure of an insulating film including a carbon film, a silicon nitride film, or a silicon oxynitride film is used.

[0199]

Furthermore, a sealing material 4509 is provided on the passivation film 4508, and a cover member 4510 is attached to. As the sealing material 4509, UV-curable resin may be used, and it is effective to provide a material having moisture-absorption effect or a material having an antioxidant effect inside. Furthermore, in the present embodiment, as the cover member 4510, a glass substrate, a quartz substrate, or a plastic substrate (including a plastic film) with a carbon film (preferably, a diamond-like carbon film) formed on both sides thereof is used.

[0200]

The light-emitting device thus manufactured is fully designed for a large area without decreasing an aperture ratio in the pixel portion.

[0201]

Note that, the present embodiment can be arbitrarily combined with either of Embodiment 1 to 6.

[0202]

[Embodiment 12]

Applying the present invention, a wiring board formed according to the present invention can be used for various electro-optic apparatuses (active matrix type liquid crystal display device, active matrix type EC display apparatus, and

active matrix type light-emitting device). Specifically, the present invention can be carried out in all the electronic equipment in which these electro-optic apparatuses are incorporated into a display portion.

[0203]

Examples of such electronic equipment include a personal computer, a display, and the like. FIG. 20 shows examples thereof.

[0204]

FIG. 20A shows a personal computer, which includes a body 3001, an image input part 3002, a display part 3003, a keyboard 3004, and the like. The present invention is applicable to the display part 3003. The present invention is ready for enlargement of the display part 3003.

[0205]

FIG. 20B shows a player using a recording medium storing a program (hereinafter, merely referred to as a recording medium), which includes a body 3401, a display part 3402, a speaker part 3403, a recording medium 3404, an operation switch 3405, and the like. Note that, this player uses a digital versatile disk (DVD), a compact disk (CD), and the like as a recording medium, and can be used for listening to music, seeing movies, playing games, and performing the Internet. The present invention is applicable to the display part 3402. The present invention is ready for enlargement of the display part 3402.

[0206]

FIG. 20C shows a display, which includes a body 4101, a support 4102, a display part 4103, and the like. The present invention is applicable to the display part 4103. The display of the present invention, especially, has a structure that is fully ready for enlargement of a screen. In particular, the present invention is advantageous for a display of 10 inches or more in the opposite angle (particularly, 30 inches or more).

[0207]

As described above, the range of application of the present invention is extremely large and the present invention is applicable to various fields of electronic

equipment. Furthermore, electronic equipment of the present embodiment can be realized by adopting the constitution using any combination of Embodiments from 1 to 11.

[0208]

[Effect of the Invention]

By adopting the constitution of the present invention, the basic significance as shown below can be obtained:

(a) a simple method suitable for processes of manufacturing conventional wiring or wiring board;

(b) low-resistance of wiring can be realized; therefore, a degree of design freedom and an aperture ratio in a pixel portion can be enhanced;

(c) satisfactory coverage can be obtained; and

(d) in a semiconductor device, typical example of an active matrix type liquid crystal display device, satisfying the above-mentioned advantages, the area of a pixel portion is enlarged, and the present invention can be fully ready for enlargement of a screen.

[Brief Description of the Drawings]

[FIGs. 1] Diagrams showing an exemplary concept of the present invention.

[FIGs. 2] Diagrams showing an exemplary shape of wiring produced according to the present invention.

[FIGs. 3] Diagrams schematically showing the shape of wiring produced according to the present invention.

[FIGs. 4] Diagrams showing an exemplary shape of wiring produced according to the present invention.

[FIGs. 5] Diagrams showing an exemplary shape of wiring produced according to the present invention.

[FIGs. 6] Diagrams showing an exemplary shape of wiring produced according to the present invention.

[FIGs. 7] Diagrams showing an exemplary concept of the present invention.

[FIGs. 8] Cross-sectional views illustrating processes of manufacturing a pixel TFT and a TFT of a driving circuit.

[FIGs. 9] Cross-sectional views illustrating processes of manufacturing a pixel TFT and a TFT of a driving circuit.

[FIG. 10] A Cross-sectional view showing processes of manufacturing a pixel TFT and a TFT of a driving circuit.

[FIG. 11] A top view showing a configuration of a pixel TFT.

[FIG. 12] A cross-sectional view illustrating processes of manufacturing an active matrix type liquid crystal display device.

[FIG. 13] A cross-sectional view illustrating processes of manufacturing an active matrix type liquid crystal display device.

[FIG. 14] A cross-sectional structural view of a driving circuit and a pixel portion of a light-emitting device.

[FIGs. 15] (A) A top view of a light-emitting device.

(B) A cross-sectional structural view of a driving circuit and a pixel portion of the light-emitting device.

[FIG. 16] A cross-sectional structural view of a driving circuit and a pixel portion of a light-emitting device.

[FIGs. 17] Diagrams showing an exemplary concept of the present invention.

[FIGs. 18] Cross-sectional views illustrating processes of manufacturing an active matrix type liquid crystal display device.

[FIG. 19] A cross-sectional structural view of a pixel portion of a light-emitting device.

[FIGs. 20] Diagrams showing examples of a semiconductor device.

[FIG. 21] A cross-sectional view illustrating processes of manufacturing a pixel TFT and a TFT of a driving circuit.

[Name of Document]

[Summary]

[Problem] An object of the present invention is; therefore, to manufacture a wiring ready for enlargement of a pixel portion, using a low-resistant material.

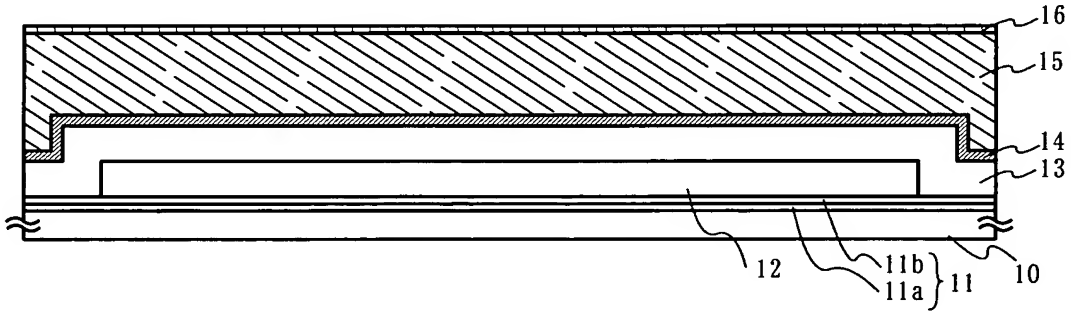
[Solving Means] The wiring of the present invention has a layered structure including a first conductive layer that has a first width and made of one or a plurality of kinds of elements selected from W and Mo, or an alloy or compound mainly containing said element as a first layer, a low-resistant second conductive layer that has a second width smaller than said first width and made of an alloy or a compound mainly containing Al as a second layer, and a third conductive layer that has a third width smaller than said second width and made of an alloy or compound mainly containing Ti as a third layer. With this constitution, the present invention is fully ready for enlargement of a pixel portion. At least edges of the second conductive layer have a taper-shaped cross-section. Because of this shape, satisfactory coverage can be obtained.

[Selected drawing] FIG. 1

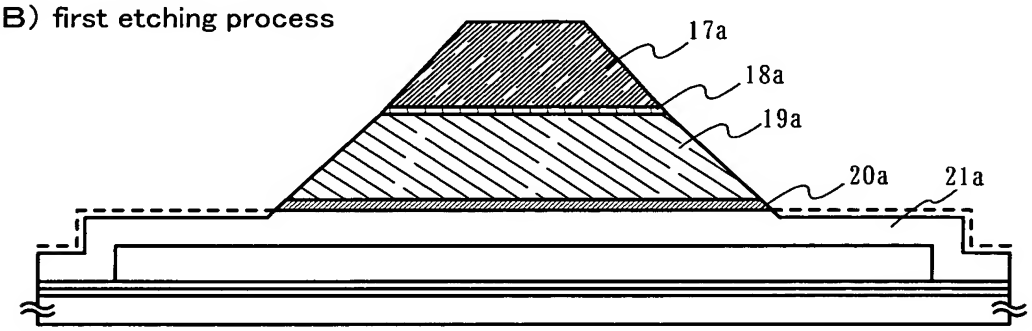
【Name of Document】 Drawings

【FIG. 1】

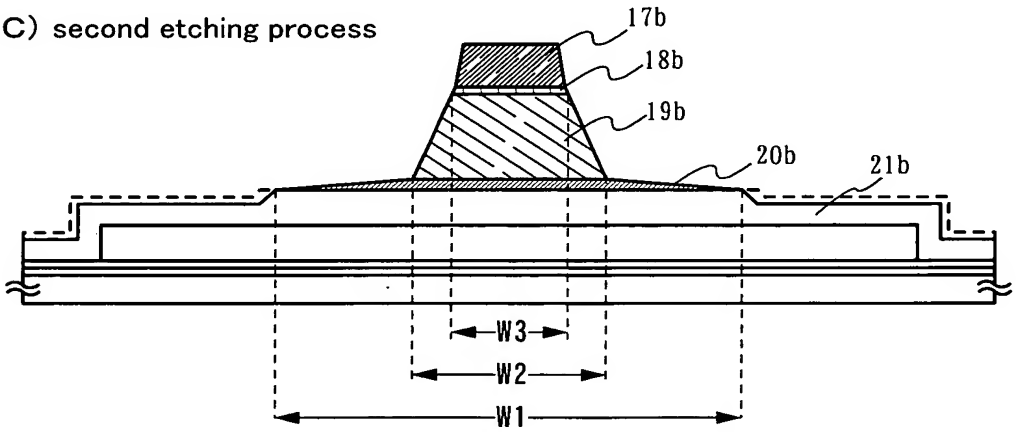
(A) forming semiconductor layer, insulating layer and first, second and third conductive layer



(B) first etching process

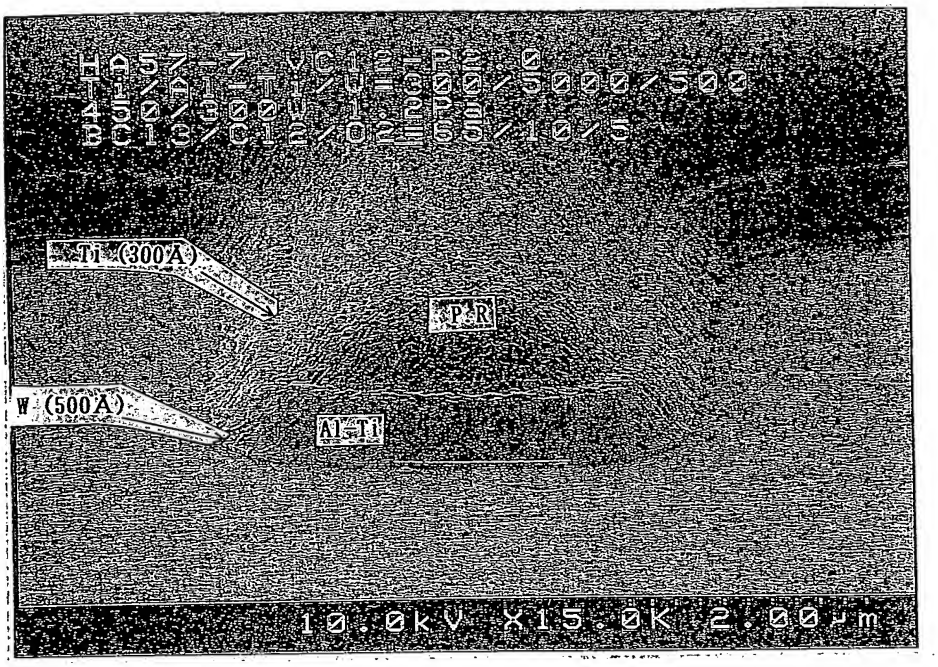


(C) second etching process

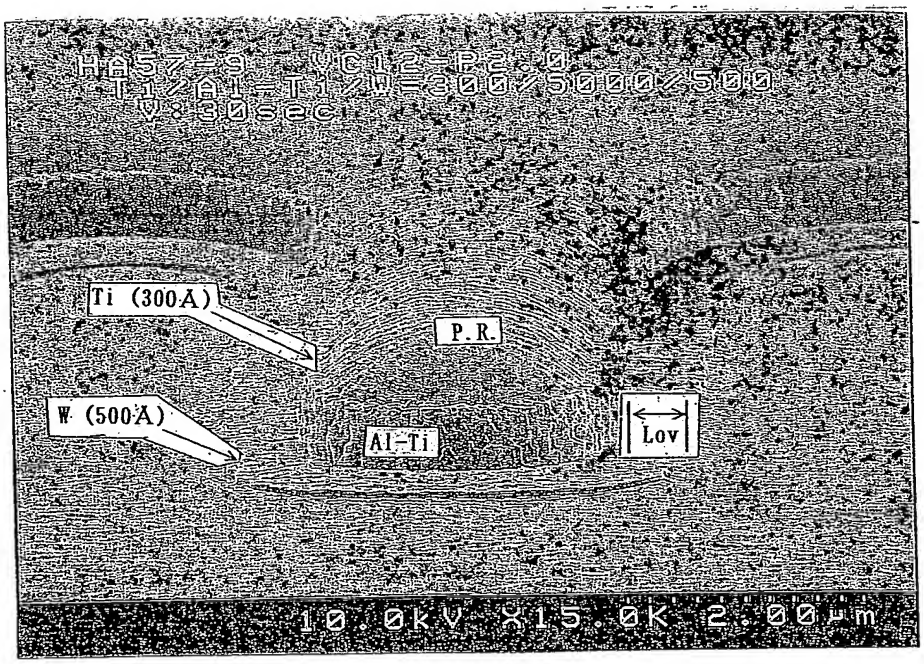


【FIG. 2】

(A)

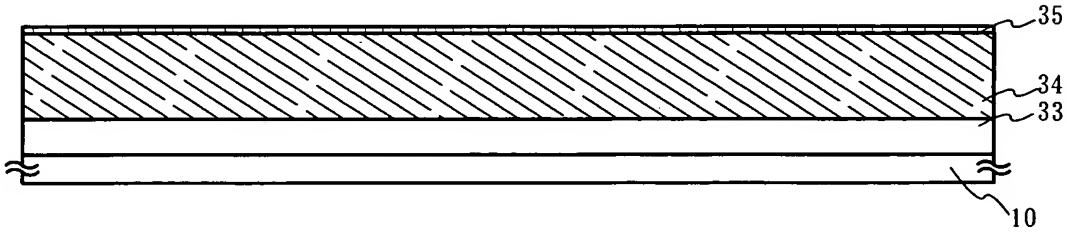

Ti (300Å)
P.R
W (500Å)
Al-Ti
10.0kV X15.0K 2.00μm

(B)

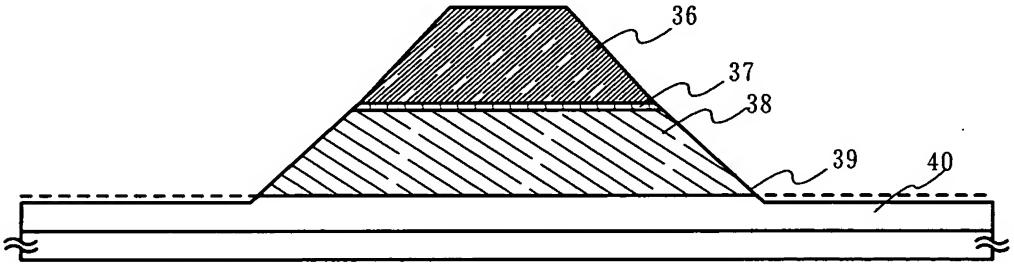

Ti (300Å)
P.R.
W (500Å)
Al-Ti
Lov
10.0kV X15.0K 2.00μm

【FIG. 3】

(A) forming insulating layer and first and second conductive layer

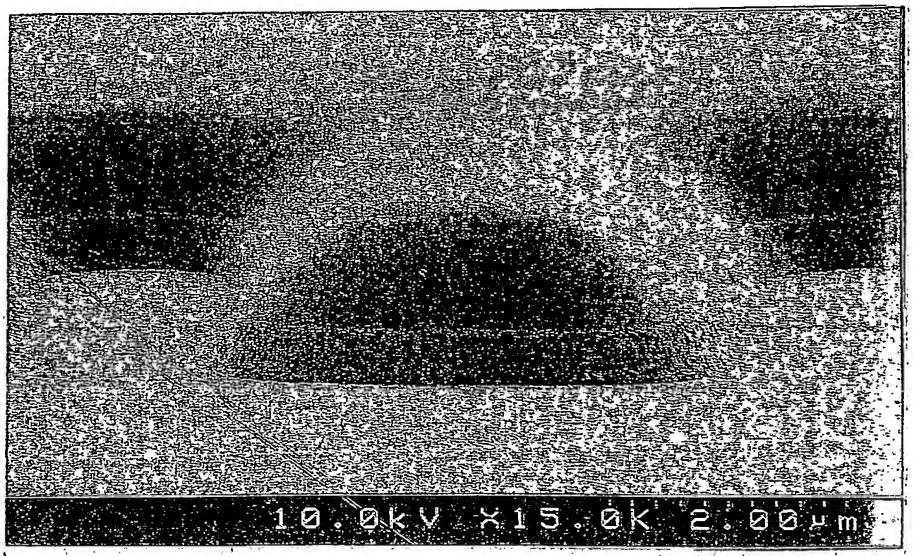


(B) etching process

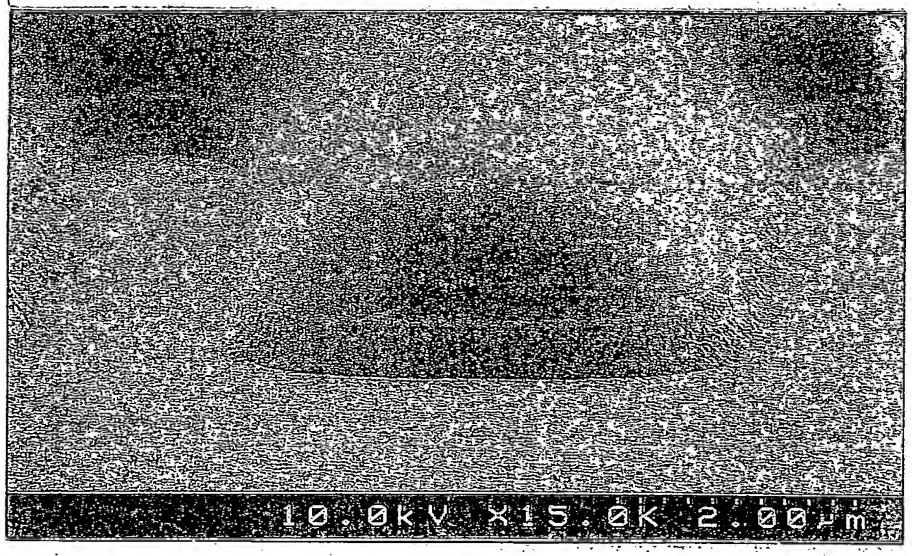


【FIG. 4】

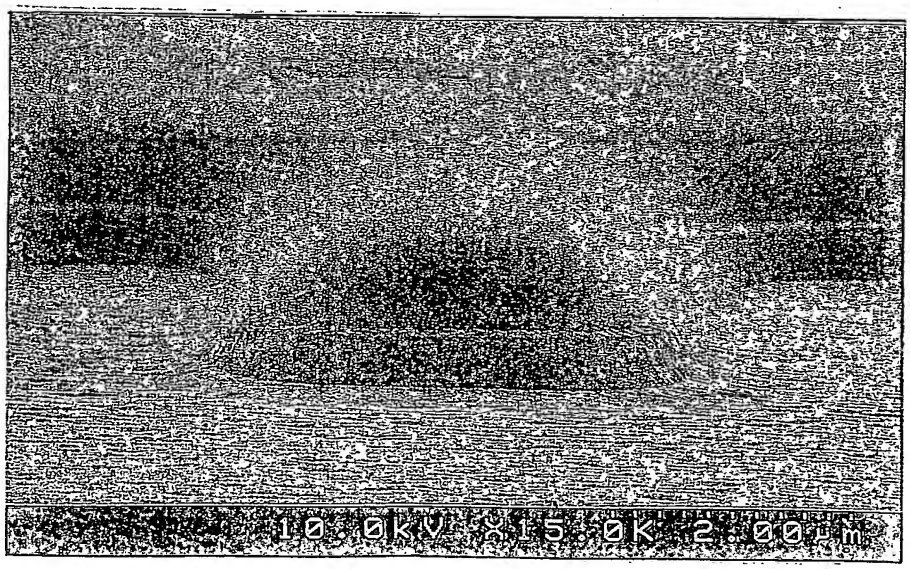
(A)



(B)

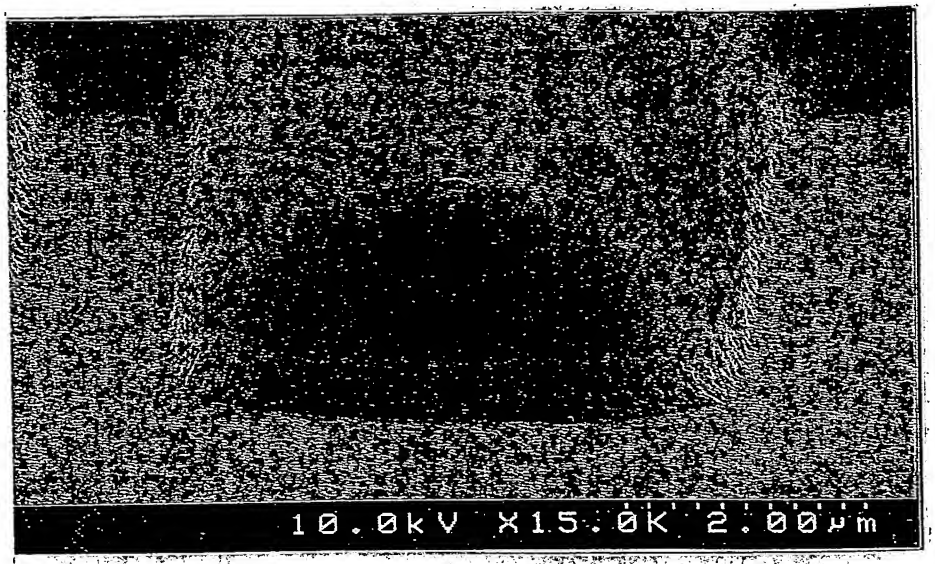


(C)

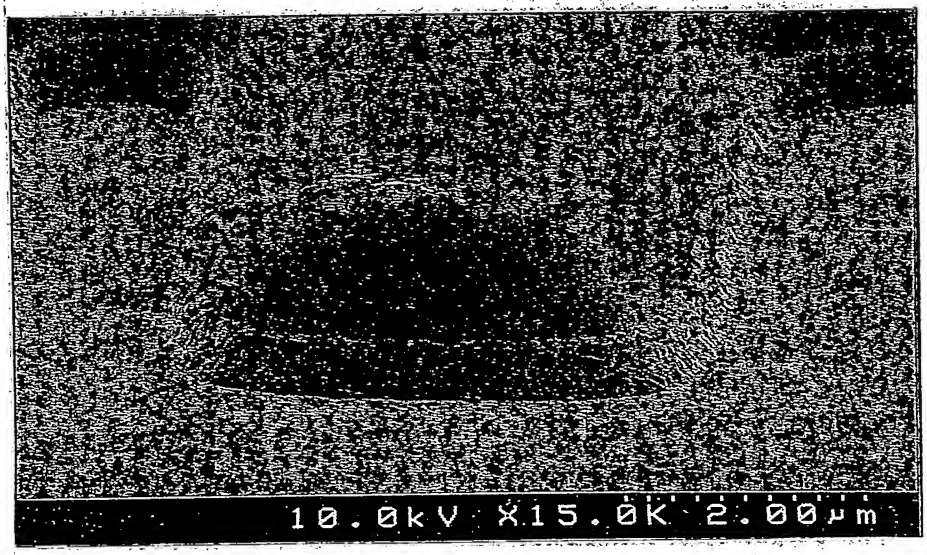


【FIG. 5】

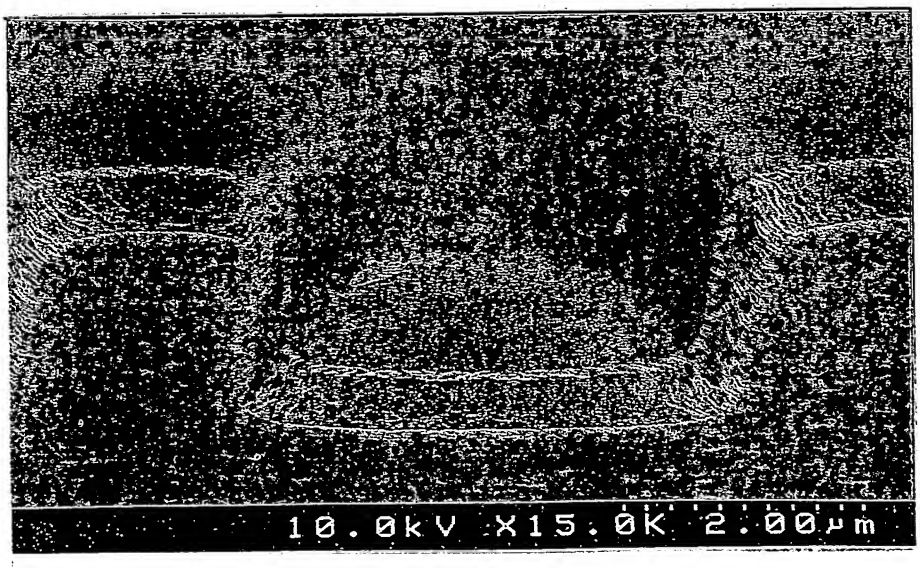
(A)



(B)

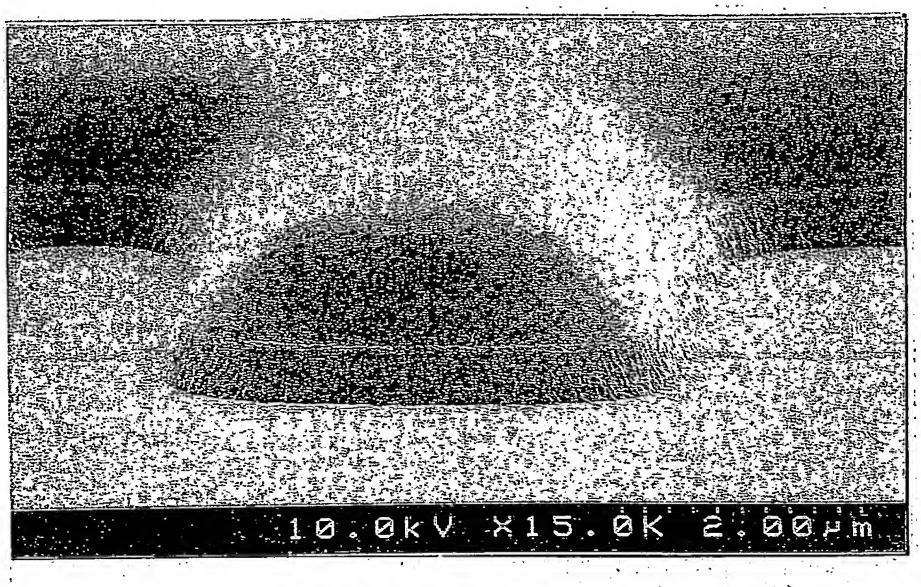


(C)

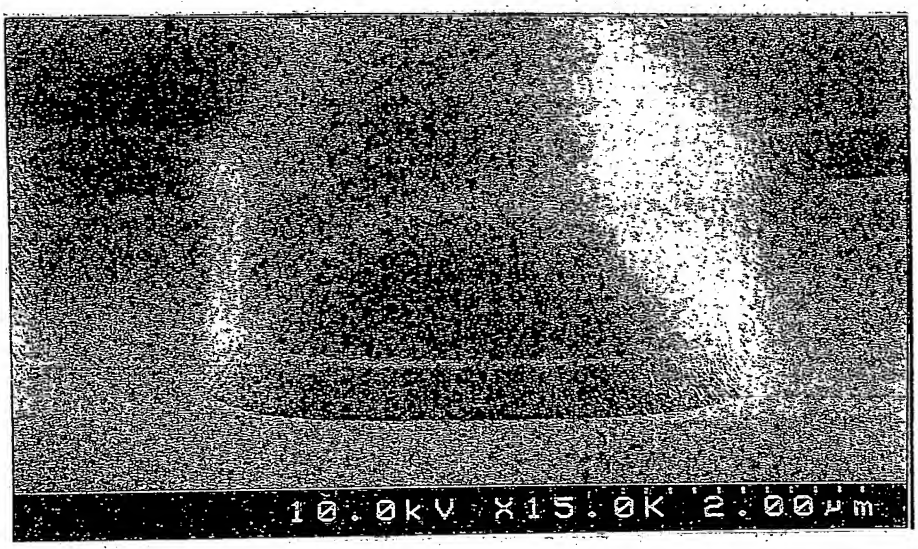


【FIG. 6】

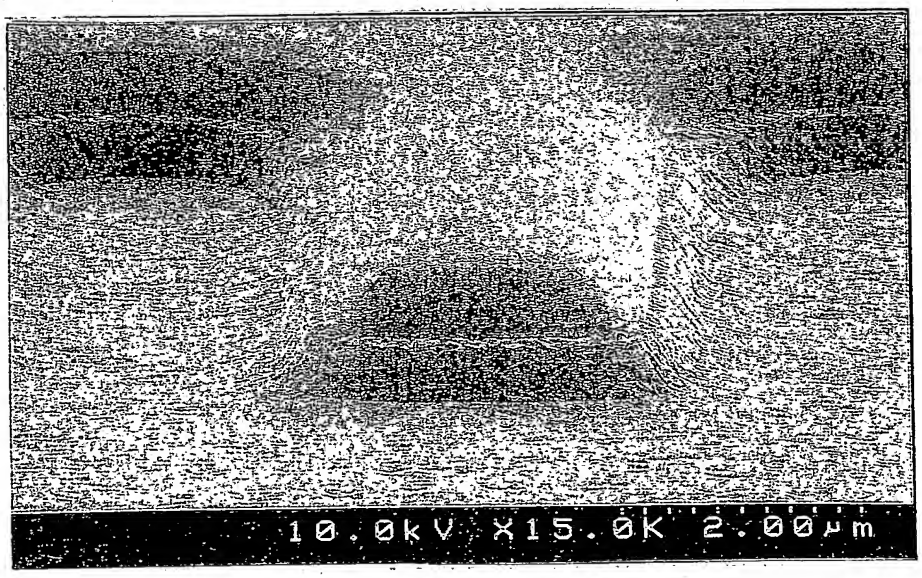
(A)



(B)

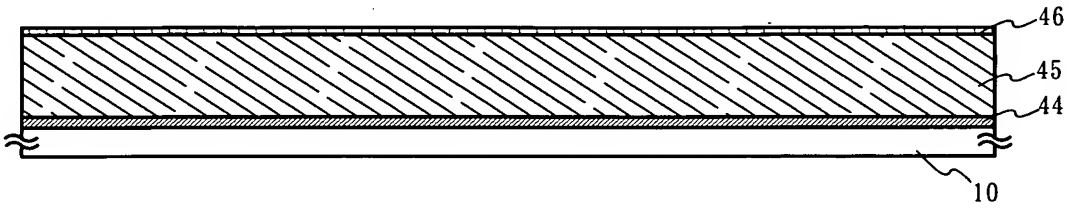


(C)

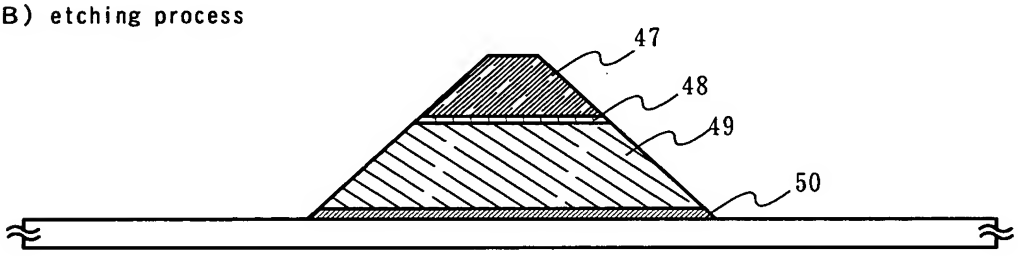


【FIG. 7】

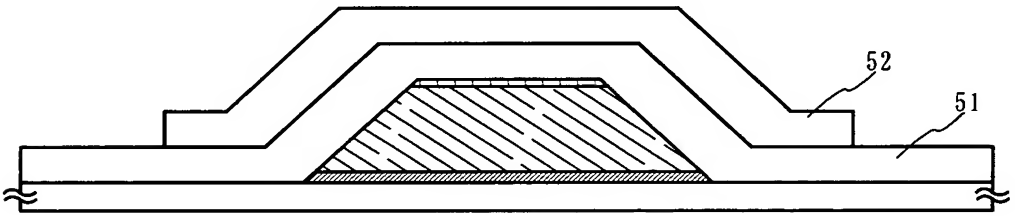
(A) fjorming first, second and third conductive layer



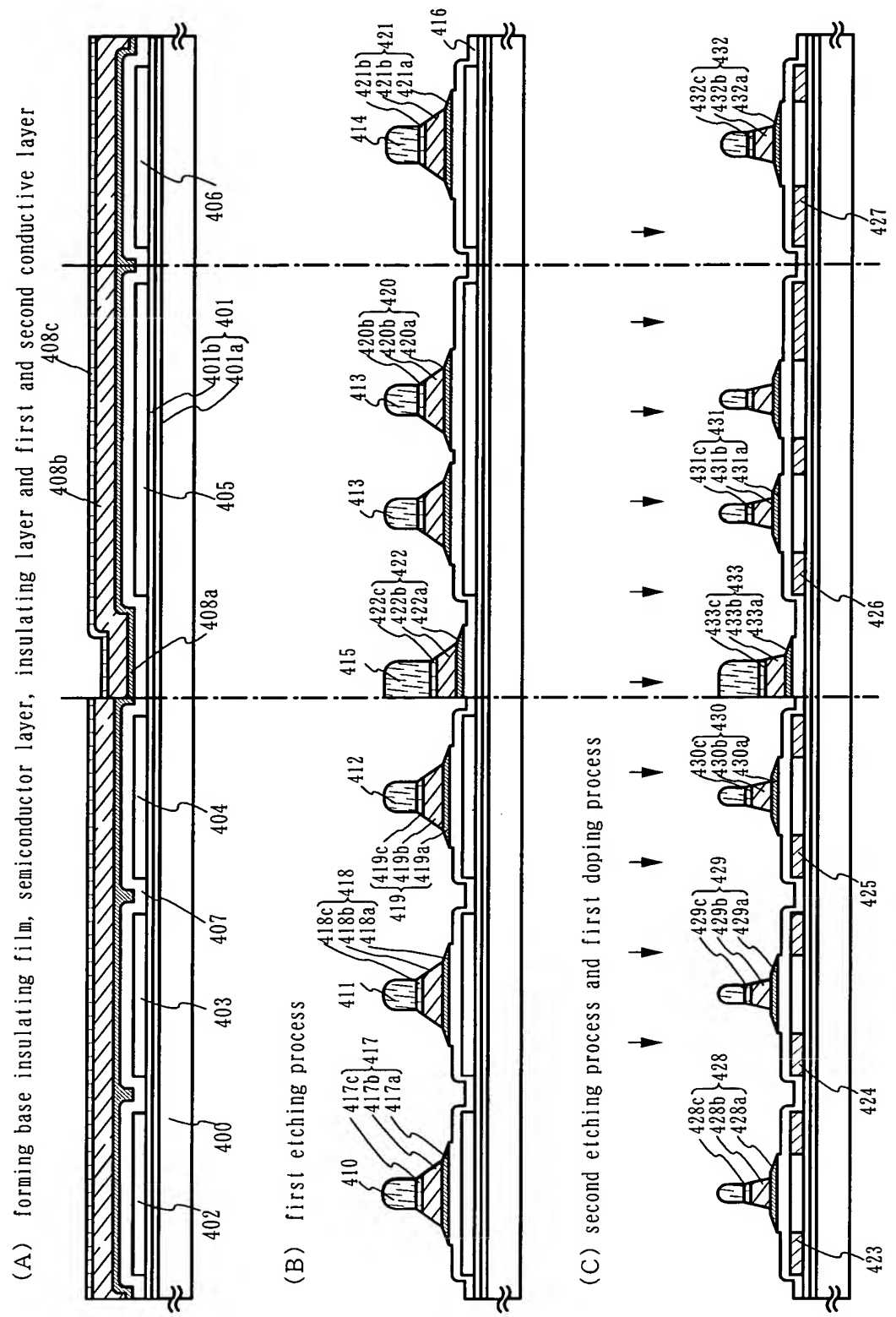
(B) etching process



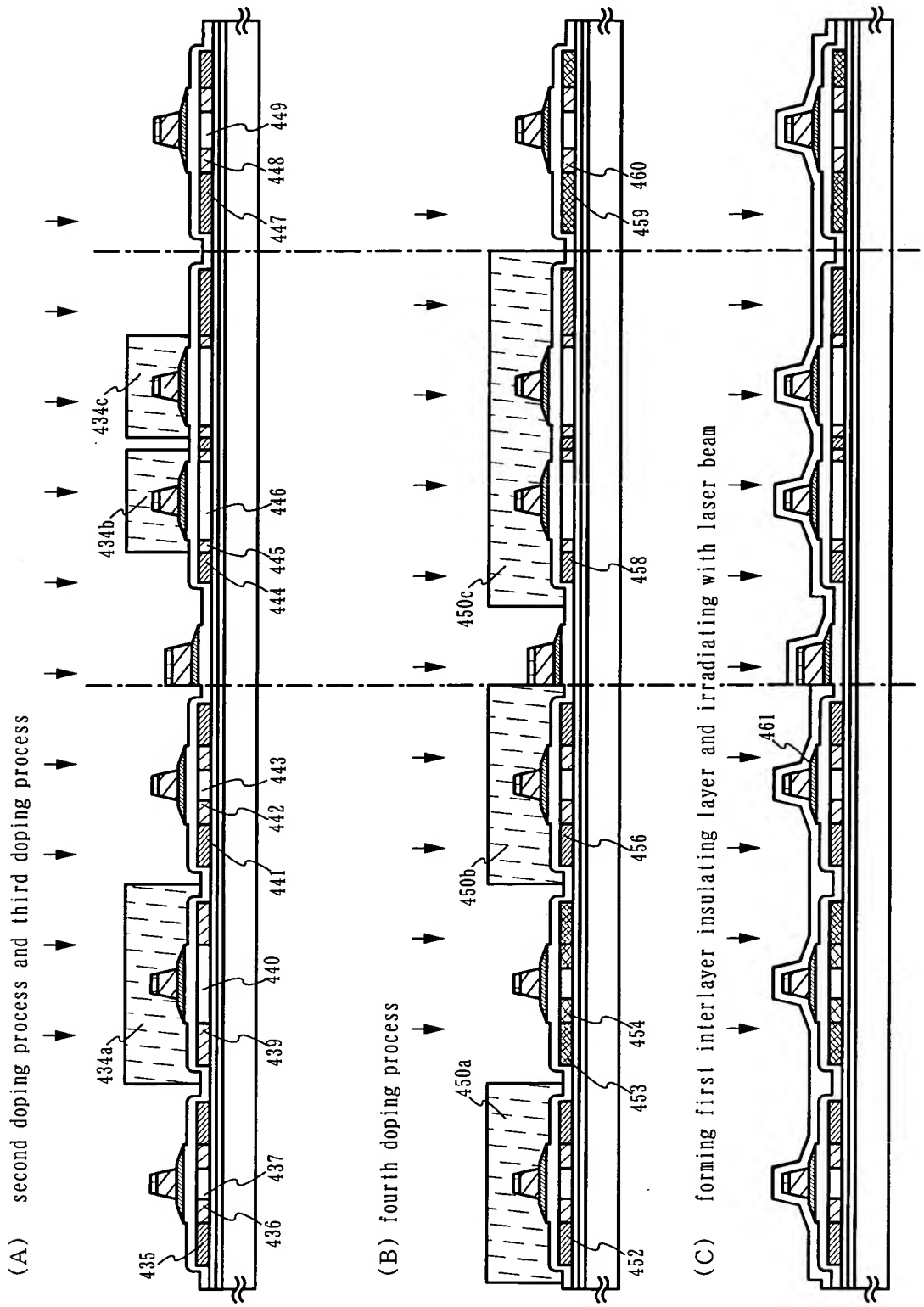
(C) forming insulating film and semiconductor film



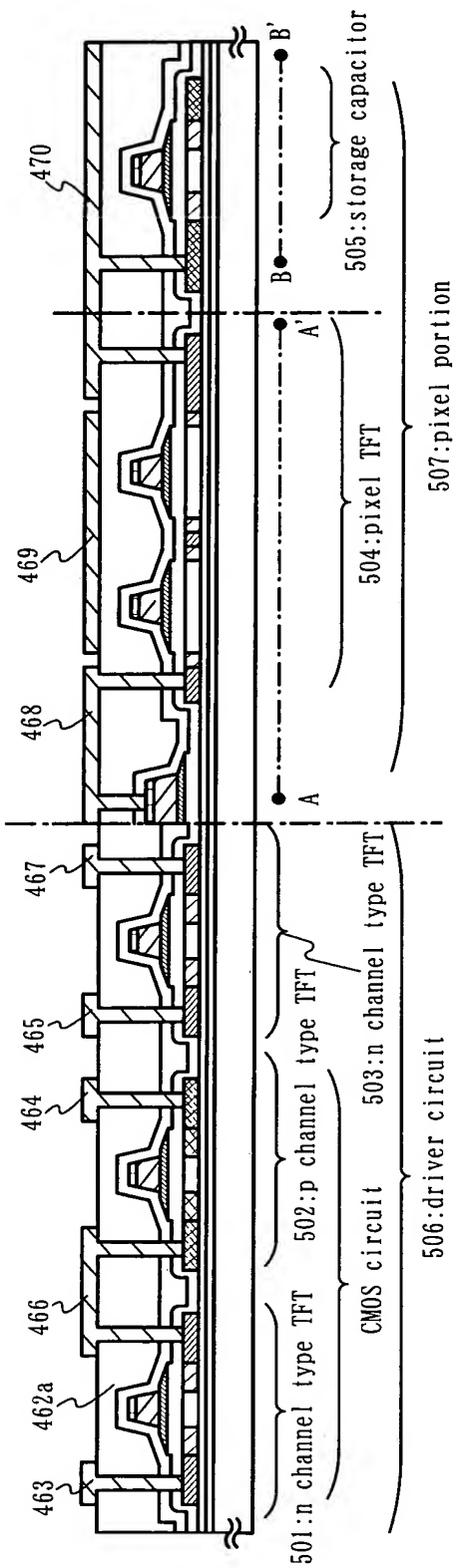
【FIG. 8】


(A) forming base insulating film, semiconductor layer, insulating layer and first and second conductive layer
(B) first etching process
(C) second etching process and first doping process
402
400
403
404
407
408a
408b
408c
405
406
401
401a
401b
410
411
412
413
414
415
416
417
417a
417b
417c
418
418a
418b
418c
419
419a
419b
419c
420
420a
420b
421
421a
421b
422
422a
422b
422c
423
424
425
426
427
428
428a
428b
428c
429
429a
429b
429c
430
430a
430b
430c
431
431a
431b
431c
432
432a
432b
432c
433
433a
433b
433c

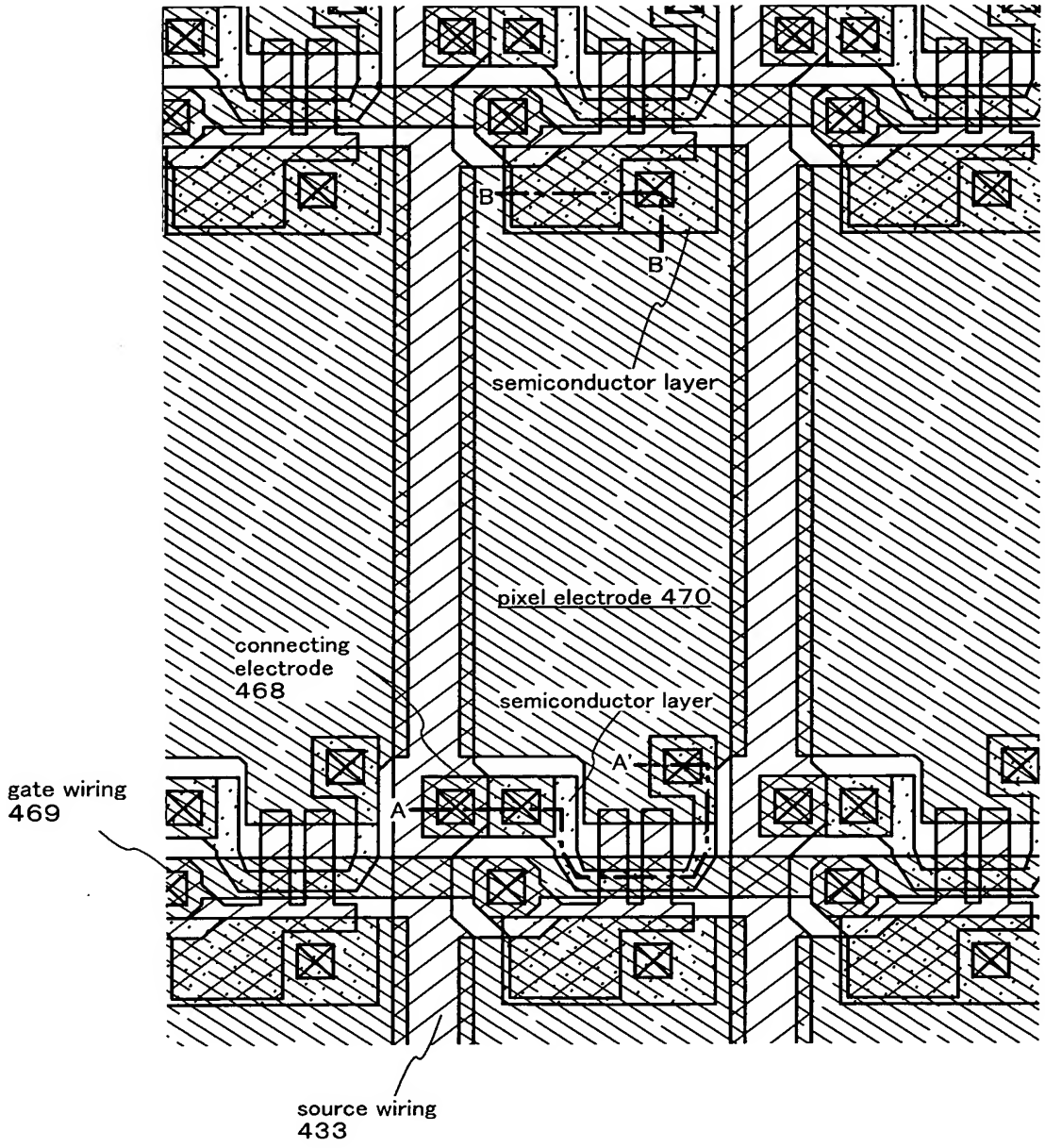
【FIG. 9】


(A) second doping process and third doping process
(B) fourth doping process
(C) forming first interlayer insulating layer and irradiating with laser beam
435
436
437
439
440
441
442
443
444
445
446
447
448
449
434a
434b
434c
450a
450b
450c
452
453
454
456
458
459
460
461

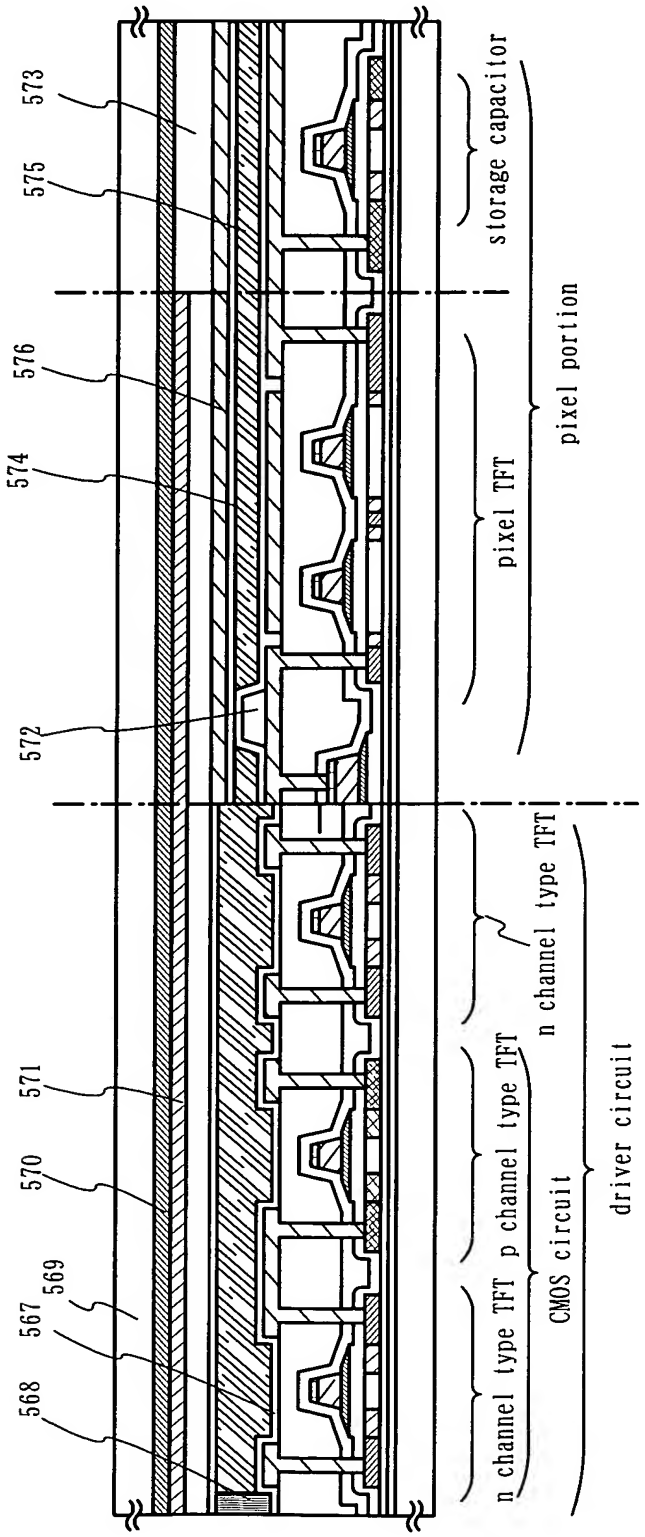
【FIG. 10】


B'
B
A'
A
505:storage capacitor
504:pixel TFT
507:pixel portion
506:driver circuit
CMOS circuit
501:n channel type TFT
502:p channel type TFT
503:n channel type TFT
470
469
468
467
465
464
466
462a
463

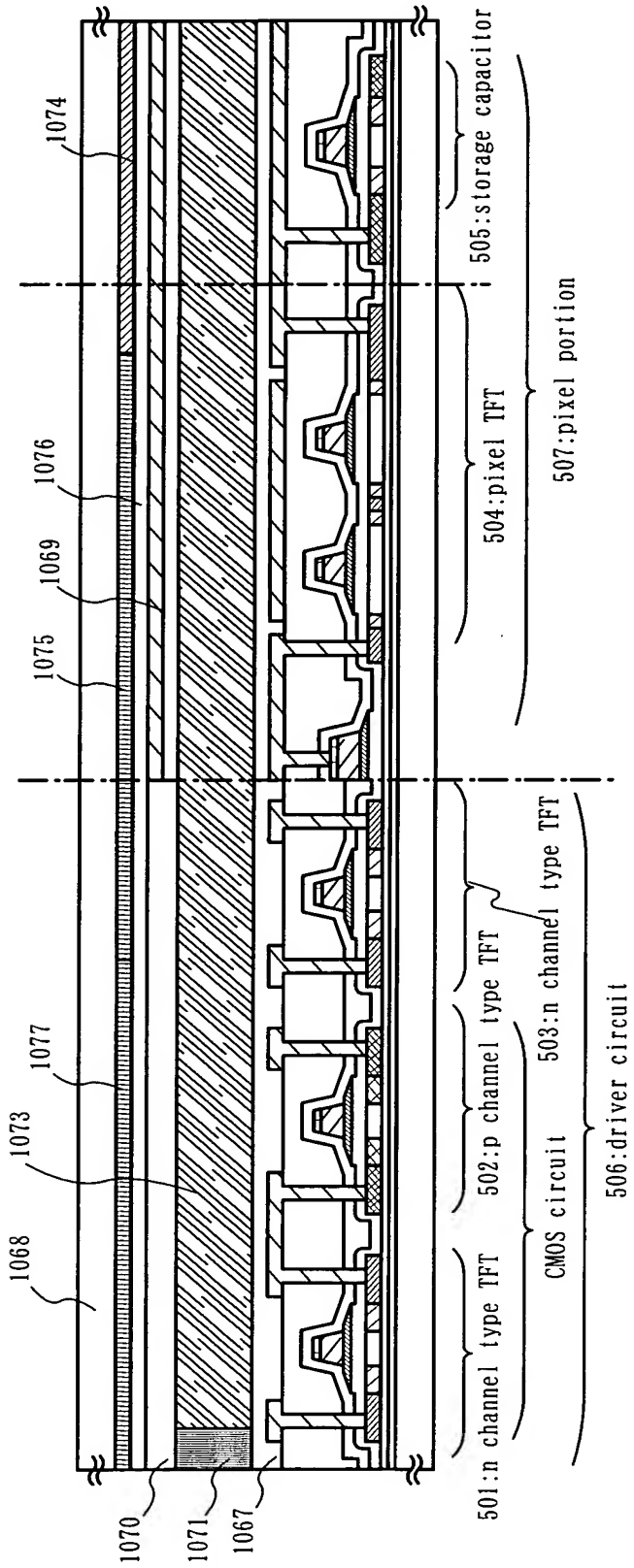
【FIG. 11】


B
B'
semiconductor layer
pixel electrode 470
connecting electrode 468
semiconductor layer
A'
A
gate wiring 469
source wiring 433

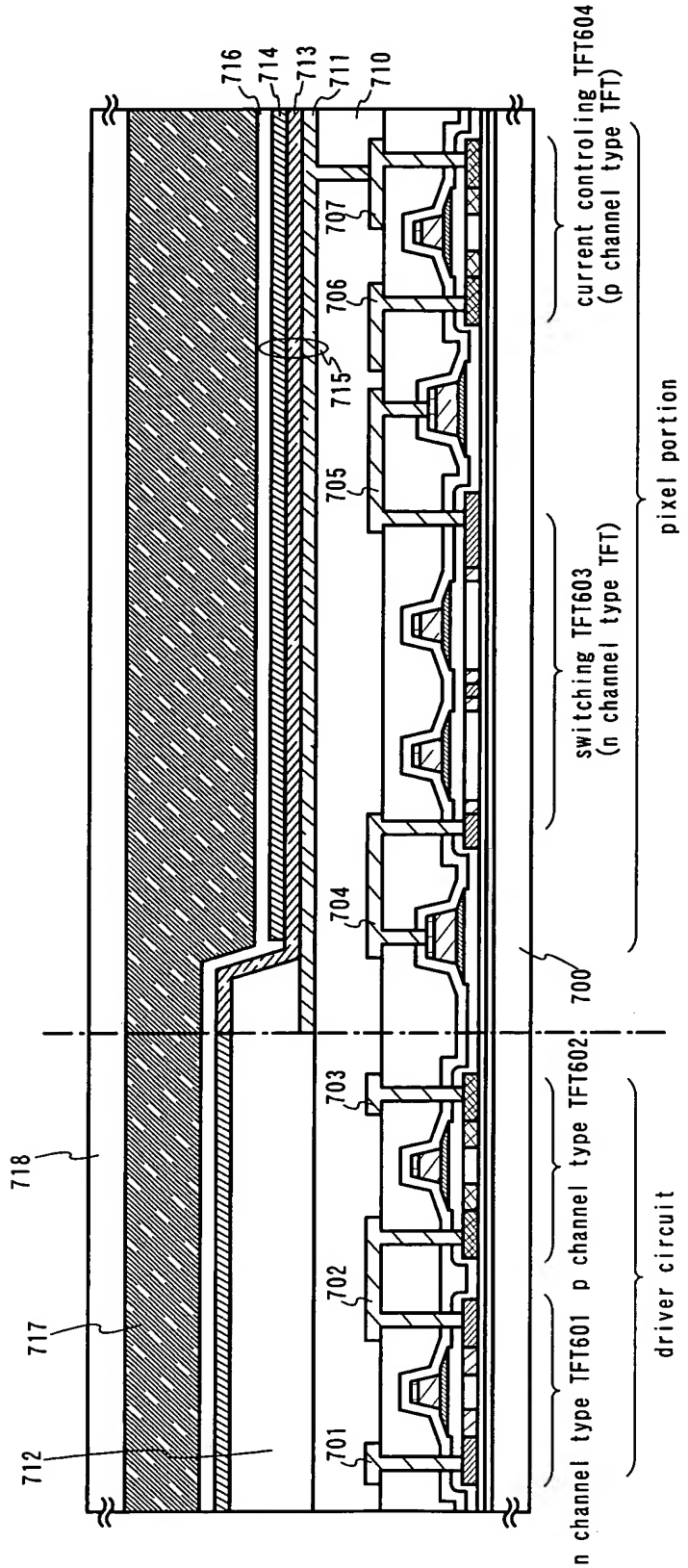
【FIG. 12】


573
575
576
574
572
571
570
569
567
568
storage capacitor
pixel TFT
pixel portion
n channel type TFT
p channel type TFT
n channel type TFT
CMOS circuit
driver circuit

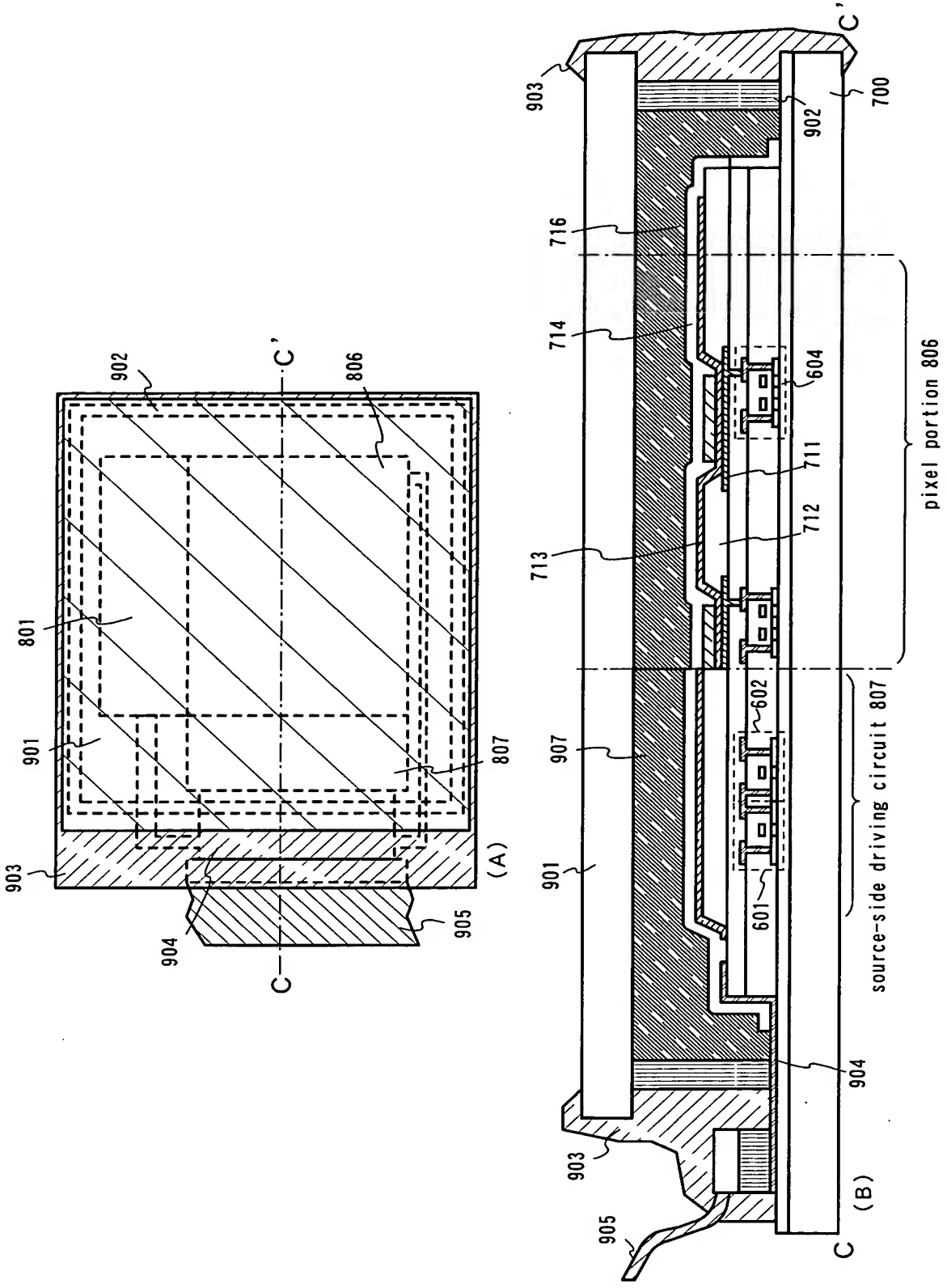
【FIG. 13】


1074
1076
1069
1075
1077
1073
1068
1070
1071
1067
505:storage capacitor
504:pixel TFT
507:pixel portion
502:p channel type TFT
503:n channel type TFT
CMOS circuit
506:driver circuit
501:n channel type TFT

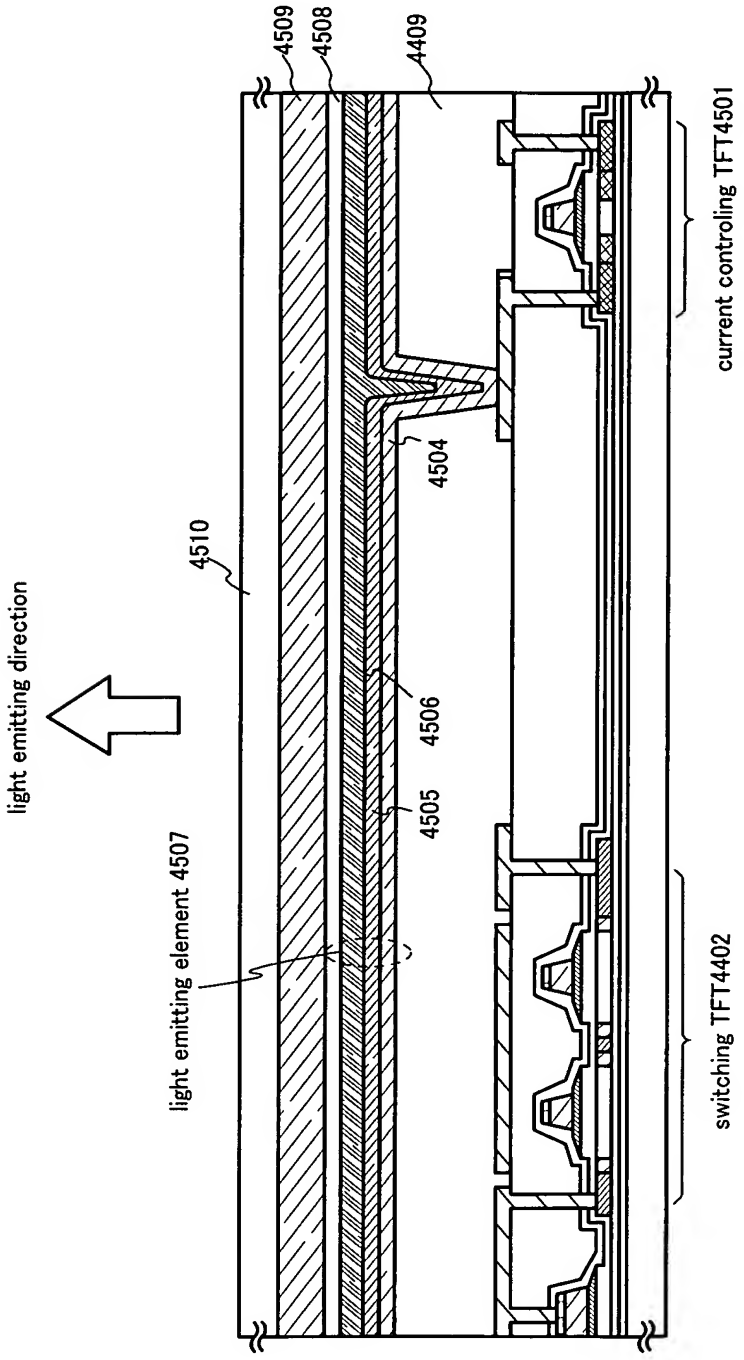
【FIG. 14】


716
714
713
711
710
707
706
715
705
704
703
702
701
718
717
712
700
current controling TFT604
(p channel type TFT)
switching TFT603
(n channel type TFT)
pixel portion
n channel type TFT601 p channel type TFT602
driver circuit

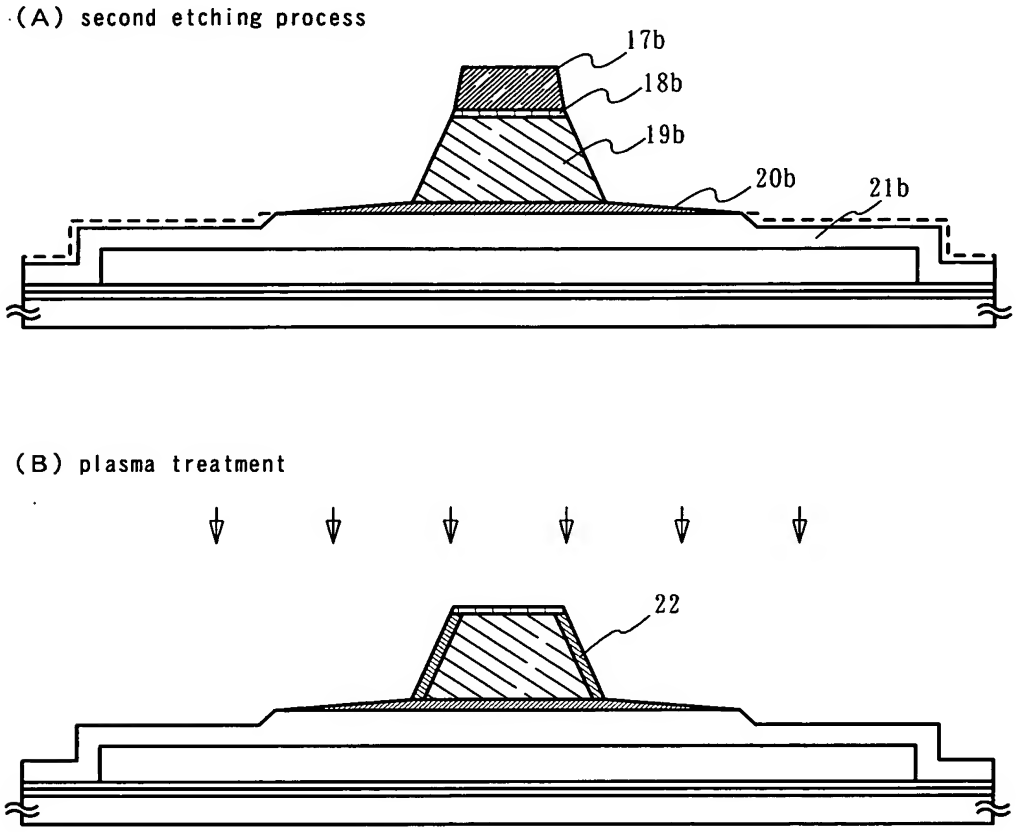
【FIG. 15】


C'
902
806
801
901
807
903
(A)
905
904
C
903
902
700
716
714
604
711
712
713
pixel portion 806
602
907
source-side driving circuit 807
901
601
904
903
905
(B)
C

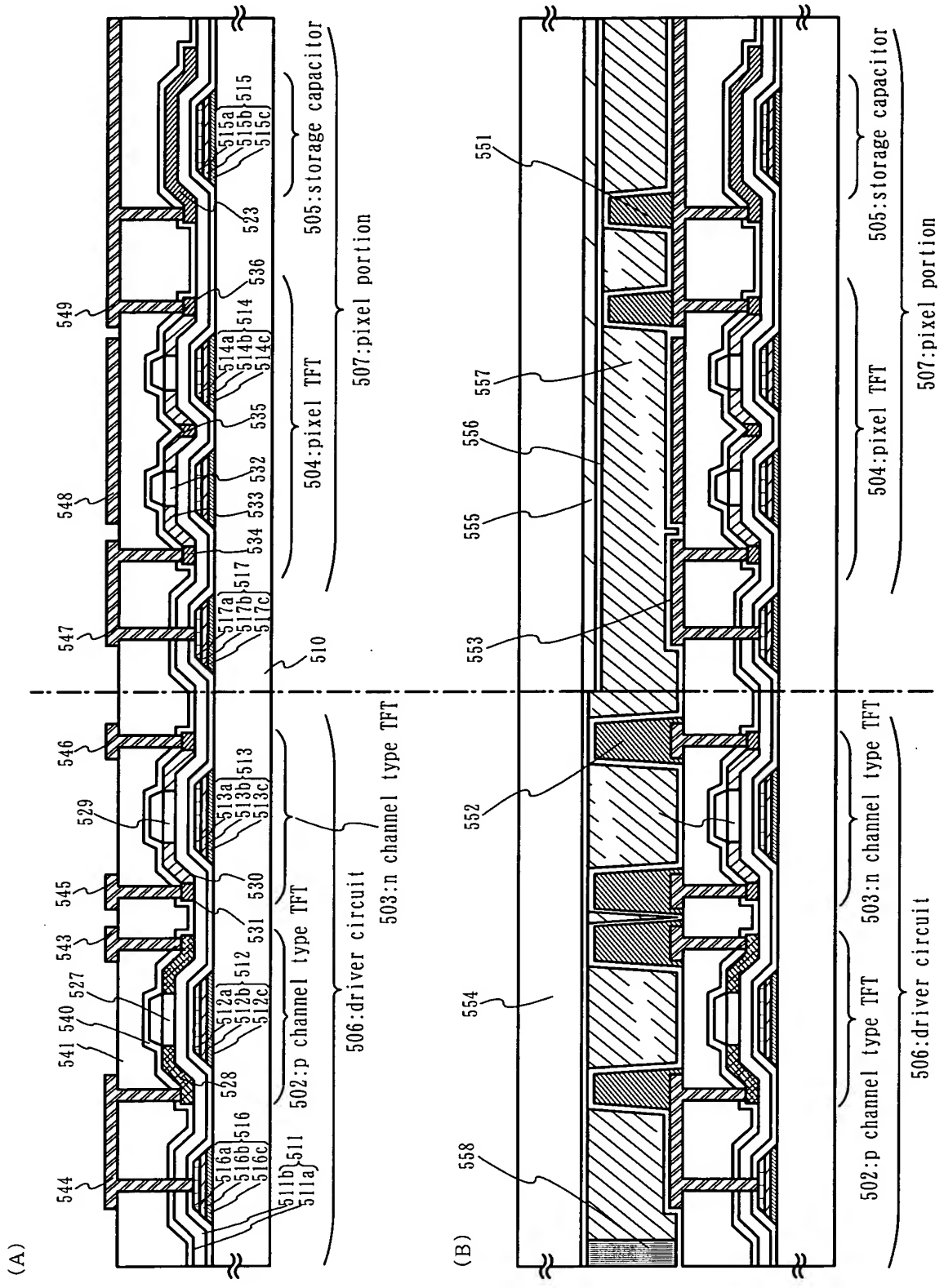
【FIG. 16】


4509
4508
4409
current controling TFT4501
4504
4510
light emitting direction
4506
4505
light emitting element 4507
switching TFT4402

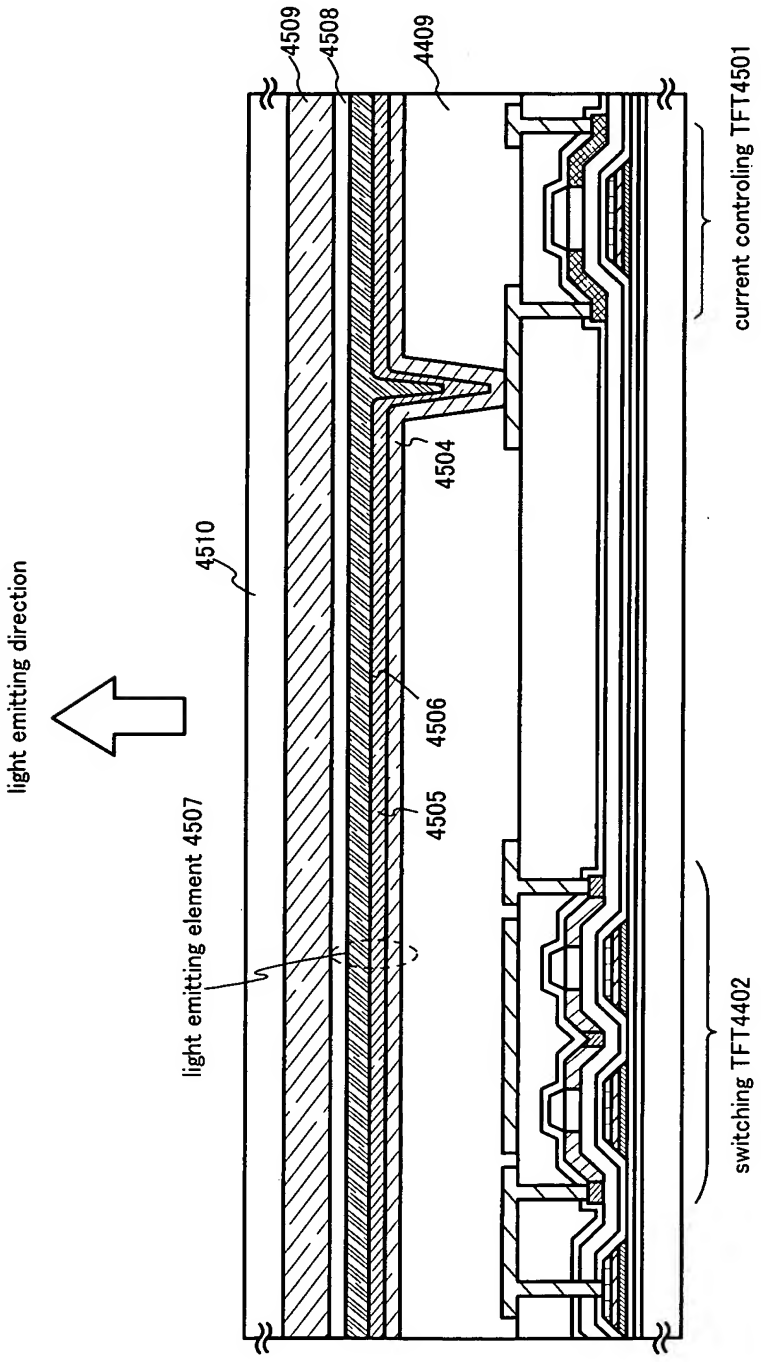
【FIG. 17】


(A) second etching process
17b
18b
19b
20b
21b
(B) plasma treatment
22

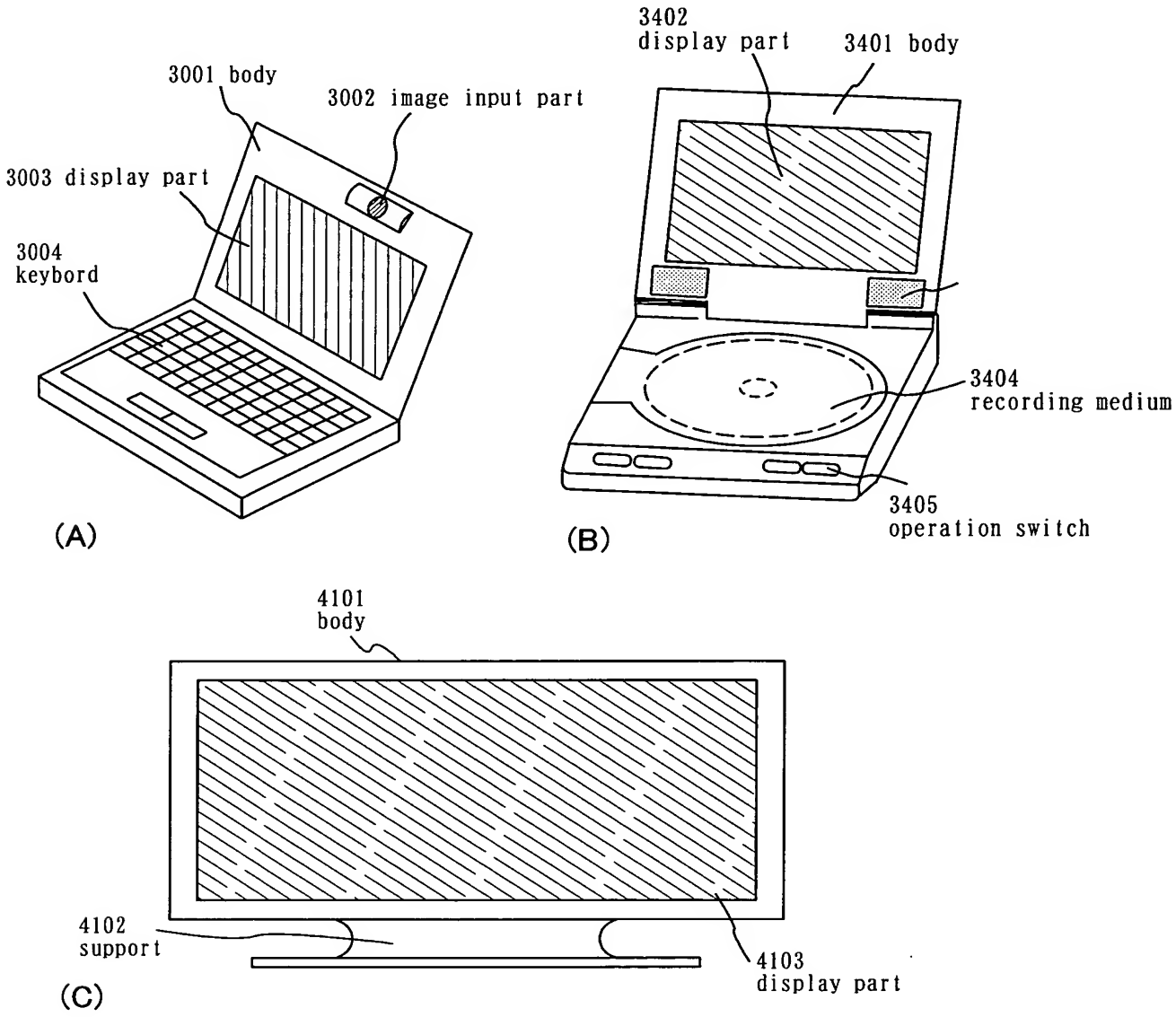
【FIG. 18】


(A)
(B)
505:storage capacitor
504:pixel TFT
507:pixel portion
502:p channel type TFT
503:n channel type TFT
506:driver circuit
549
548
547
546
545
544
543
529
527
541
540
528
516
511
510
523
536
535
532
533
534
517
513
530
531
512
515
514
551
557
556
555
553
552
554
558

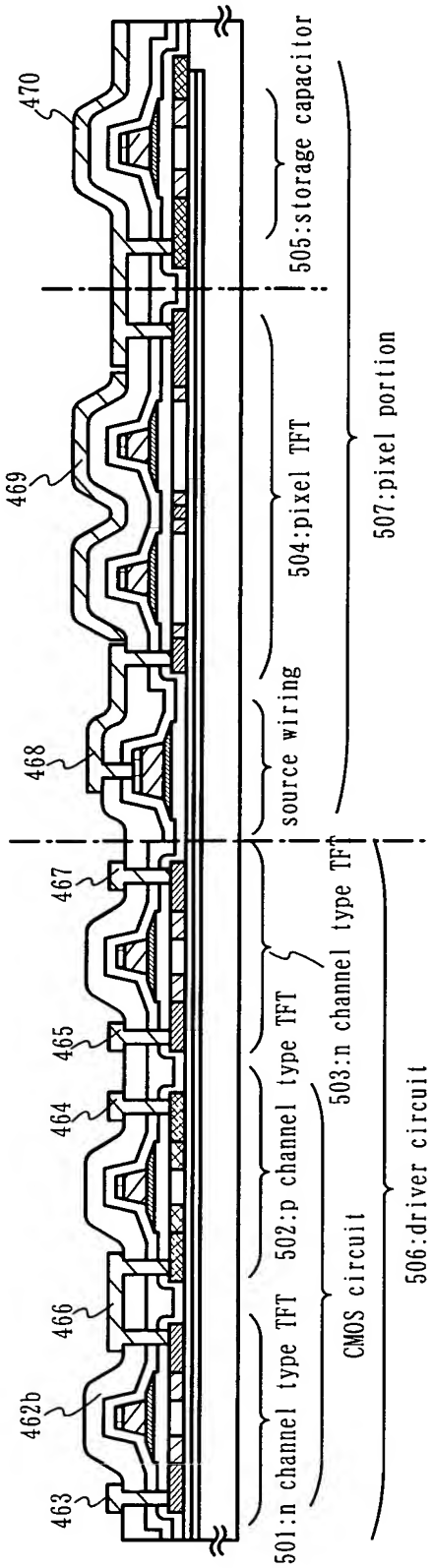
【FIG. 19】


4509
4508
4409
current controling TFT4501
4504
4510
light emitting direction
4506
4505
light emitting element 4507
switching TFT4402

【FIG. 20】


3001 body
3002 image input part
3003 display part
3004
keybord
(A)
3402
display part
3401 body
3404
recording medium
3405
operation switch
(B)
4101
body
4102
support
4103
display part
(C)

【FIG. 21】


470
469
468
467
465
464
466
462b
463
505:storage capacitor
504:pixel TFT
source wiring
507:pixel portion
503:n channel type TFT
502:p channel type TFT
CMOS circuit
501:n channel type TFT
506:driver circuit